Development of Plasma-based Atom Selective Etching: A Novel Polishing Technique for Single-Crystal Materials

A thesis

Submitted to The School of Engineering at The University of East Anglia in Partial Fulfillment of The Requirements for The Degree of

DOCTOR OF PHILOSOPHY

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September 2021

Abstract

Polishing difficult-to-machine single-crystal materials, such as SiC, is very time-consuming and difficult to achieve atomic-level damage-free surface. To address this problem and provide a potential solution to fabricate truly-atomically flat surfaces, a novel polishing technique called plasma-based atom selective etching (PASE) is proposed in this thesis. PASE featuring ultrahigh polishing precision could outpace the state-of-the-art polishing method: chemical mechanical polishing (CMP). In this research, the material removal rate of PASE is thousands of times higher than that of CMP. The fast polishing of single-crystal material can be realized by selectively removal atoms which form the roughness and leave behind the integral perfect single-crystal basement. The underlying mechanism of PASE is based on the difference in the chemical reactivity of atoms at different sites and aims to maximize the difference using proper reaction conditions. Ab initio molecular dynamics (AIMD) simulations have been performed to explore the mechanism. Several prototype machines with the optimal plasma nozzle and torch have been developed throughout the experimental tests. Experiments and characterizations have been conducted to optimize the parameters of PASE and verify the speculated mechanism. To demonstrate the advantages of PASE, many difficult-to-machine materials, including SiC, GaN, Si, Al_2O_3, and AlN, have been investigated; in particular, SiC is discussed extensively. It is noted that a sliced SiC with a roughness over 100 nm has been successfully reduced to the atomic level (Ra ~ 0.05 nm) within 5 minutes by an ultrahigh material removal rate of ~ 30 μm/min. Furthermore, broader applications of PASE, including dislocation detection and subsurface damage measurement, have been provided to demonstrate its technological advance.

Acknowledgement

I would first like to thank the Shenzhen government, SUSTech, and UEA, who provided the financial support and gave me the chance to do this PhD project.

I would express my sincere gratitude to my supervisors: Dr Hui Deng and Dr Dianzi Liu, who gave me the PhD topic, taught me how to do experiments, helped me polish my articles, and always gave me valuable advice when I was confused. I am also grateful to Professor Yiming Rong for accepting my PhD application.

I would like to thank the collaborators: Mr Kaixuan Gu for cooperating with me for the simulation part of this project; Dr Khan Muhammad Ajmal for helping me in revising the English grammar and polishing my articles; Dr Yuanming Zhu for his assistance at SUSTech Core Research Facilities. I would also like to thank the group members, including Dr Hu Luo, Dr Jianwei Ji, Mr Zejing Zhan, Ms Fang Wang, Ms Rong Yi, Mr Nian Liu, Mr Linfeng Zhang, Mr Rulin Li, Mr Wang Liu, Mr Shaoxiang Liang and Ms Yanan Liang, for their accompany throughout these four years.

Many thanks to my friends. Mr Sining He, Ms Xian Li, Mr Zongyong Zhang, Mr Yufan Hui and Dr Chengyang Liu, for the weekends we spent together cooking in the UK. Thanks to my undergraduate classmates, Mr Changliang Peng, Ms Yuan Shi, and Mr Wenxuan Hu, who kept in touch with me during the PhD and shared their everyday stories. Very special thanks to the friends in my hometown, Mr Kangdi Hu, Mr Chun Jiang, Mr Huang Li, Mr Anbang Huang, Ms Feiyan Li, Ms Feilu Jiang, and Ms Xi He; coming back to the hometown and playing with you during the vacations has always been a comfort during the hard times.

Finally, my parents deserve endless gratitude for their support and encouragement.

Publications

1. **Y. Zhang,** K. Gu, L. Zhang, Y. Zhu, D. Liu, H. Deng, A generic ultrafast polishing method with truly-atomic flatness. (Under review)

2. **Y. Zhang**, Y. Hu, D. Liu, H. Deng, PASE polishing of sapphire. (Under review)

3. **Y. Zhang**, L. Zhang, K. Cheng, D. Liu, D. Lu, H. Deng, Rapid subsurface damage detection of SiC using inductivity coupled plasma, *International Journal of Extreme Manufacturing*, 3 (2021) 035202.

4. Z. Fang#, **Y. Zhang#**, R. Li, Y. Liang, H. Deng, An efficient approach for atomic-scale polishing of single-crystal silicon via plasma-based atom-selective etching, *International Journal of Machine Tools and Manufacture*, 159 (2020) 103649.

5. **Y. Zhang#**, H. Chen#, D. Liu, H. Deng, High efficient polishing of sliced 4H-SiC (0001) by molten KOH etching, *Applied Surface Science*, (2020) 146532.

6. **Y. Zhang**, R. Li, Y. Zhang, D. Liu, H. Deng, Indiscriminate revelation of dislocations in single crystal SiC by inductively coupled plasma etching, *Journal of the European Ceramic Society*, 39 (2019) 2831-2838.

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9. Y. Zhang, S. Liang, **Y. Zhang**, R. Li, Z. Fang, S. Wang, H. Deng, Role of oxygen in surface kinetics of SiO2 growth on single crystal SiC at elevated temperatures, *Ceramics International*, 47 (2020) 1855-1864.

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Abbreviations

2D	Two Dimensional
4H-SiC	Silicon Carbide With 4h Polytype
a.u.	Atomic Units
ACSM	Atomic And Close-To-Atomic Scale Manufacturing
AEPM	Arc-Enhanced Plasma Machining
AFM	Atomic Force Microscopy
AIMD	Ab-Initio Molecular Dynamics
AP	Atmospheric Pressure
APPP	Atmospheric Pressure Plasma Polishing
BC	Before Christ
BPDs	Basal Plane Dislocations
CARE	Catalyst-Referred Etching
CCP	Capacitive Coupled Plasma
CLSM	Confocal Laser Scanning Microscopy
CMP	Chemical Mechanical Polishing
CMRF	Chemical Magnetorheological Finishing
CNY	Chinese Yuan Renminbi
CZ method	Czochralski method
DFTB	Density Functional Based Tight Binding
e.g.	Exempli Gratia (meaning: for example)
EBE	Electron Beam Evaporation

EBE	Electron Beam Evaporated
EBID	Electron Beam Induced Deposition
EBID	Electron-Beam Induced Deposition
ECMP	Electro-Chemical Mechanical Polishing
EDS	Energy-Dispersive X-Ray Spectroscopy
EEM	Elastic Emission Machining
EPD	Etching Pits Density
et al.	Et Alia (meaning: and others)
etc.	Et Cetera (meaning: and so on)
EUV	Extreme Ultraviolet
FCC	Face-Centered Cubic
FIB	Focused Ion Beam
FIB	Focused Ion Beam
GBP	British Pound Sterling
HRTEM	High Resolution Transmission Electron Microscopy
IBF	Ion Beam Figuring
IBID	Ion Beam Included Deposition
IBID	Ion-Beam Included Deposition
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
ICP-MS	Inductively Coupled Plasma - Mass Spectrometry
ICP-OES	Inductively Coupled Plasma - Optical Emission Spectrometry
IOM	Leibniz Institute of Surface Modification
KMC	Kinetic Monte Carlo
LCMP	Laser-Assisted Chemical Mechanical Polishing

MFC	Mass Flow Controller
MOSFET	Metal Oxide Semiconductor Field Effect Transistors
MR	Magnetorheological
MRF	Magnetorheological Finishing
MRR	Material Removal Rate
NAZ	Normal Analysis Zone
NC	Numerical Control
OES	Optical Emission Spectrometry
PAP	Plasma Assisted Polishing
PASE	Plasma-Based Atom Selective Etching
PCMP	Photocatalytic-Assisted Chemical Mechanical Polishing
PCVM	Plasma Chemical Vaporization Machining
PEEK	Polyether ether ketone
PJM	Plasma Jet Machining
PSD	Power Spectral Density
PTFE	Poly Tetra Fluoroethylene
PV	Peak-To-Valley
Ra	Roughness Average (Arithmetical Mean Height of a Line)
RAPT	Reactive Atom Plasma Technology
RB-SiC	Reaction-Bonded Silicon Carbide
RF	Radio Frequency
RMS	Root Mean Square
RMSD	Root Mean Square Displacement/Deviation
Sa	The Extension of Ra to a Surface
SAED	Selected Area Electron Diffraction

SB	Single Bilayer
SCCM	Standard Centre Cubic Per Minute
SE	Step-Edge
SEM	Scanning Electron Microscopy
SLM	Standard Liter Per Minute
SSD	Subsurface Damage
S-SiC	Sliced SiC
ST	Step Terrace
STEM	Scanning Transmission Electron Microscopy
STM	Scanning Tunneling Microscope
TCP	Tribochemical Polishing
TEDs	Threading Edge Dislocations
TEM	Transmission Electron Microscopy
TSDs	Threading Screw Dislocations
TTV	Total Thickness Variation
UCMP	Ultrasonic-Assisted Chemical Mechanical Polishing
UHV	Ultrahigh Vacuum
WBG	Wide Bandgap
XPS	X-Ray Photoelectron Spectroscopy

Chapter 1

Introduction

1.1 Motivation

The development of human civilization is constantly accompanied by the utilization of new materials and the advancement of manufacturing precision. The mainly utilized materials have been used to name the periods of civilization, from the stone edge, bronze age, to the iron age. Today, people are in the age of information, which is also called the silicon age, by many [1]. The manufacturing precision has also evolved from millimeter to micrometer and nanometer, from craft-based manufacturing tracing back to over 4000 B.C. to the automatic machinery developed since the industrial revolution [2].

The first-generation semiconductor materials represented by silicon have greatly promoted the development of the microelectronics and integrated circuit (IC) industry. Silicon is still the most widely used material in semiconductor devices and possesses the advantages of abundance in nature, well-established manufacturing, stability in room temperature, and ease to control doping and oxidization [1, 3]. However, silicon also has many limitations that restrict its application. For instance, poor electron mobility and hole mobility are barriers to silicon for higher performance [4]. Meanwhile, the moderate bandgap and low electric breakdown field limit its application for high voltage devices [5]. The low saturation drift velocity restricts the switching frequency of the silicon-based device. Furthermore, the valence electrons jump to the conduction band and cause uncontrolled conduction at high temperatures, which limits the operating temperature of the

silicon-based device to below 150°C [6]. As the silicon material approaches its limitations, new materials with better performance are highly desired. The idea of wide bandgap (WBG) materials, which is also referred to as the third-generation semiconductor material, has been proposed to break the limitations of silicon [7]. Single crystal silicon carbide (4H-SiC) has attracted significant attention as one of the most promising WBG materials owing to its superior electrical, mechanical, and chemical properties. 4H-SiC has is especially suitable for producing devices that operate under high voltage, high switching frequency, and high-temperature conditions due to the wide bandgap, high breakdown field, high thermal conductivity, and strong chemical inertness [8-10]. To fabricate electronic devices based on 4H-SiC, atomic flatness and damage-free surfaces are essential. However, owing to its high hardness (Mohs hardness: 9.0-9.5, Vickers Hardness: 24-28 GPa) and high chemical inertness, 4H-SiC is one of the most difficult-to-machine materials in the world [11]. Obtaining a perfect 4H-SiC surface efficiently without scratches or subsurface damage (SSD) remains a challenge. Many cutting-edge polishing methods have been proposed to achieve the high-quality and high-efficient polishing of 4H-SiC. Among them, chemical mechanical polishing (CMP) is currently the most commonly used method in industrial production. However, the drawbacks of CMP remain obvious: ultra-low material removal rate (~100 nm/min), massive consumption of slurry and polishing pads which are expensive and pollute the environment, difficulties to achieve atom-level material removal owing to the grain size, etc. The first motivation of this thesis is to find a better solution for the high-efficiency polishing of 4H-SiC and other difficult-to-machine WBG materials and facilitate the development of the next-generation devices.

The second motivation is to pursuit the limit of manufacturing precision. Modern lithography enables the fabrication of devices with 3 nm resolution, and ion beam finishing (IBF) can achieve sub-nanometer accuracy [12]. What is the next stage of manufacturing precision? Fang concludes the next phase of manufacturing as atomic and close-to-atomic scale manufacturing (ACSM), where

the material removal, transformation, and addition are at atomic precision [2]. The ACSM methods available today are still very limited. One of the essential fields of ACSM is the manufacturing of a truly-atomically flat surface, which means ideally, all atoms within the surface are in the same layer of crystal plane. It is also known as the roughness limit of a surface in the field of applied physics [13]. Many state-of-the-art methods have been invented to get close to this goal. However, due to machine tool precision, cutting tool interaction with the workpiece, and low atomic manipulation efficiency, fabricating large-scale surfaces with atomic-level precision is still challenging [2]. Developing the state-of-the-art method to advance the precision of manufacturing 2D-surface to the atomic level and fabricating large-scale truly-atomically flat surfaces is the second motivation of this thesis.

In summary, two motivations for this thesis are; (i) Addressing the problem of polishing 4H-SiC and other difficult-to-machine WBG materials. (ii) Developing a state-of-the-art polishing technique to pursue polishing limits and achieve a truly-atomically flat surface. Driven by these two motivations, a novel polishing method named plasma-based atom selective etching (PASE) is proposed in this thesis. PASE is based on selective removal of atoms that result in surface roughness due to their different chemical properties than the perfect crystal plane beneath them. This polishing configuration is the most efficient; meanwhile, the selectivity is toward the atomic level. Hence PASE can achieve fast polishing of 4H-SiC and many other crystal materials with theoretically atomic precision.

1.2 Thesis organization

In this thesis, the concept of PASE has been proposed, the development of confirmatory apparatus has been described, and the mechanism speculation and simulation has been given. PASE has been confirmed as a novel ultra-fast polishing method that can achieve atomic flatness. It could replace the polishing and ultra-precision polishing techniques in wafer manufacturing if a high temperature and uniform etchant-gas environment could be obtained. The immediate application of

dislocation detection and SSD detection using PASE has also been discussed.

Chapter 1 introduced the motivation of PASE, and the significance and content of this thesis.

Chapter 2 provides an introduction to the material focused on in this study. Then, a literature review of the current ultra-precision polishing method and methods to achieve a truly-atomically flat surface has been presented. The merits and demerits of those methods have been summarized. Finally, the concept of PASE is proposed to solve the problems of the aforementioned methods.

Chapter 3 introduces the design and built apparatuses to achieve PASE. Some preliminary experiments to help optimize the apparatus have also been presented.

Chapter 4 discusses the plasma diagnostics that were used to investigate and ensure the etching ability of plasma. The polishing effect of PASE has been experimentally confirmed. Truly-atomic roughness has been obtained, and an ultra-high material removal rate has been observed. The universality of PASE on other difficult-to-machine materials has been tested.

Chapter 5 gives the mechanism speculation based on several experiments that study the PASE parameters separately. Verification of the mechanism based on simulation has been presented.

Chapter 6 discusses the dislocation revelation and elimination phenomena during PASE. PASE has been found to be a suitable dislocation detection method when the selectivity was modified towards dislocations. The comparison between PASE and conventional molten KOH etching method for dislocation detection has been discussed.

In **Chapter 7**, the damage-free processing propriety of PASE has been utilized to do SSD detection. PASE has been proved to be a rapid SSD detection method, and the influence of several machine parameters on the SSD has been studied via

PASE.

Chapter 8 summarizes this thesis, and the perspectives for future work are discussed.

Chapter 2

Background

2.1 Third-generation semiconductor materials

Third-generation semiconductor materials, also called WBG materials, refer to semiconductors with a bandgap over 2.3 eV. They are widely used in new energy vehicles, rail transit, smart grid, new generation mobile communication, consumer electronics, and other fields and are regarded as the core technology supporting the development of energy, transportation, information, defense, and other industries [14]. The WBG materials have superior properties such as wide bandgap, high breakdown electric field, high thermal conductivity, high saturation drift velocity, and higher radiation resistance which enable it to be used in producing devices that operate under a harsh environment, including high voltage, high switching frequency, and high-temperature conditions [8-10].

WBG materials consist of group IV-IV semiconductors (SiC, diamond, etc.), group II-VI semiconductors (ZnSe, ZnO, *etc.*), group III-V nitride semiconductors (BN, AlN, GaN, InN, AlGaInN, GaNAs, GaNP, *etc.*) [15]. The development of WBG material-based platforms requires maturing in wafer production, micromachining, and material integration [16]. SiC and GaN are considered promising and are currently the only available WBG materials on the semiconductor portfolio market due to the commercial availability of wafers and outstanding properties (**Table 1**, [17]). Among them, SiC is the most established substrate because it is much cheaper than GaN, and SiC wafer production industry

is more mature [16].

Table 1 Properties of Si, SiC (4H), and GaN [17, 18].

Property	Si	SiC (4H)	GaN
Bandgap (eV)	1.12	3.26	3.45
Electron mobility ($cm^2/(V·s)$)	1500	1000	1250
Hole mobility ($cm^2/(V·s)$)	600	115	850
Breakdown field (kV/cm)	300	3000	3500
Thermal conductivity (W/(cm·K))	1.5	4.9	1.3
Saturation drift velocity (10^7 cm/s)	1	2	2.2
Intrinsic temperature (°C)	315.48	1318.35	1393.85
Vickers Hardness (GPa)	13-16	24~28	18~20

2.1.1 4H-SiC

Single crystal silicon carbide has one-dimensional polymorphism, there is an infinite number of possible SiC polytypes, and over 200 types of polytypes have been discovered [19]. Silicon and carbon atoms are bound in a tetrahedral arrangement with four neighbours due to sp^3 hybridization of Si and C, forming the basic building block of SiC as shown in **Figure 2.1(a)**. [20]. The basic tetrahedral building blocks connected edge by edge form the Si-C bilayers (**Figure 2.1(b)**). The SiC polytypes are differentiated by the repetition period of each Si-C bilayer. The naming of a SiC polytype is consists of a number and a letter (C, H, R). The letter refers to the basic crystallographic categories: cubic (C), hexagonal (H), and rhombohedral (R). And the number represents the number of bilayers included in one repetition period. **Figure 2.1(c)** shows the structure of the most commonly used SiC polytype: 3C-, 6H- and 4H-. Many SiC polytypes exist due to the slight energy differences in hexagonal and cubic crystal layers, and even small energy fluctuations could affect the crystal structure [15]. Hexagonal stacking has slightly smaller energy than cubic stacking. The energy difference can be applied from

temperature variations; for instance, high-temperature annealing can transform cubic structures into hexagonal structures [21].

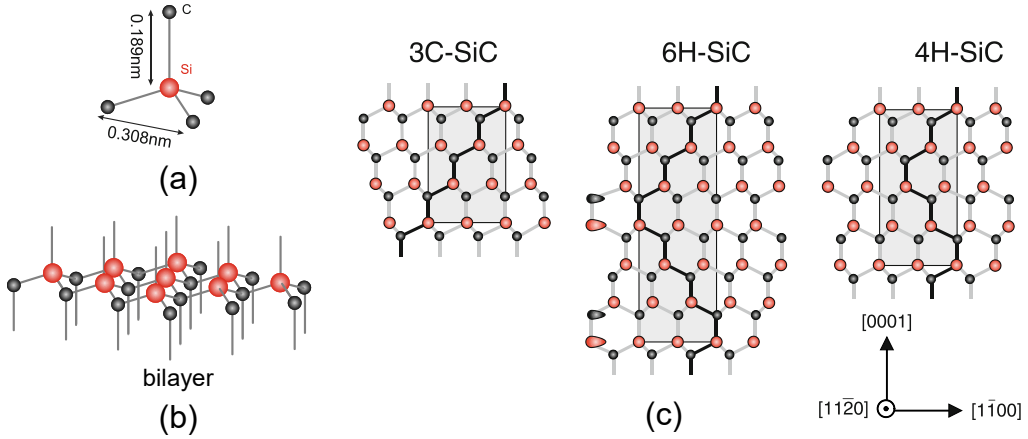


Figure 2.1 (a) basic tetrahedral building block of SiC; (b) Si-C bilayer; (c) side view projection on the (11$\bar{2}$0) plane of three different polytypes of SiC [20].

6H-SiC was the dominant polytype being researched before the introduction of the 4H-SiC wafer in 1994. Since then, 4H-SiC has gradually become a more dominant component of electronics due to the identical mobilities along the two planes of 4H-SiC, which is different for 6H-SiC [17].

Compared with silicon, the breakdown field of 4H-SiC is about ten times higher; thus, the SiC power devices can be one-tenth thinner than Si-based devices. Meanwhile, the larger handling current density can reduce the size of SiC devices. For instance, the on-resistance of SiC-based MOSFET (metal oxide semiconductor field-effect transistors) is two or more orders of magnitude smaller than that of Si-based MOSFET since the on-resistance is inversely proportional to the third power of the electric breakdown field [22]. The on-resistance causes thermal loss, which will be much smaller on Si-based MOSFET. The practical SiC-based device has a power loss of less than 1/300 of that of Si-based devices [22]. In addition, the thermal conductivity of SiC is three times higher than Si, which can simplify the cooling system can enable the application under high power working conditions. The wider bandgap results in a higher intrinsic temperature of SiC to around 1318.35°C, compared to about 315.48°C for Si, since more thermal energy is needed to move electrons in the valence band to conduction band [18]. Hence the

operation temperature of SiC-based devices can be much higher. The reduction of power loss and increased operational temperature can guarantee higher integration of high-power devices and a simpler cooling system, which offers a promising approach for miniaturization of high power and high-frequency equipment.

2.1.2 Wafer manufacturing process

The manufacturing of SiC devices can be divided into wafer manufacturing, front-end process, and back-end process, as shown in **Figure 2.2**. This study focuses on the wafer manufacturing process, specifically polishing and ultra-precision polishing parts. The general wafer manufacturing process consists of seven steps, as listed below.

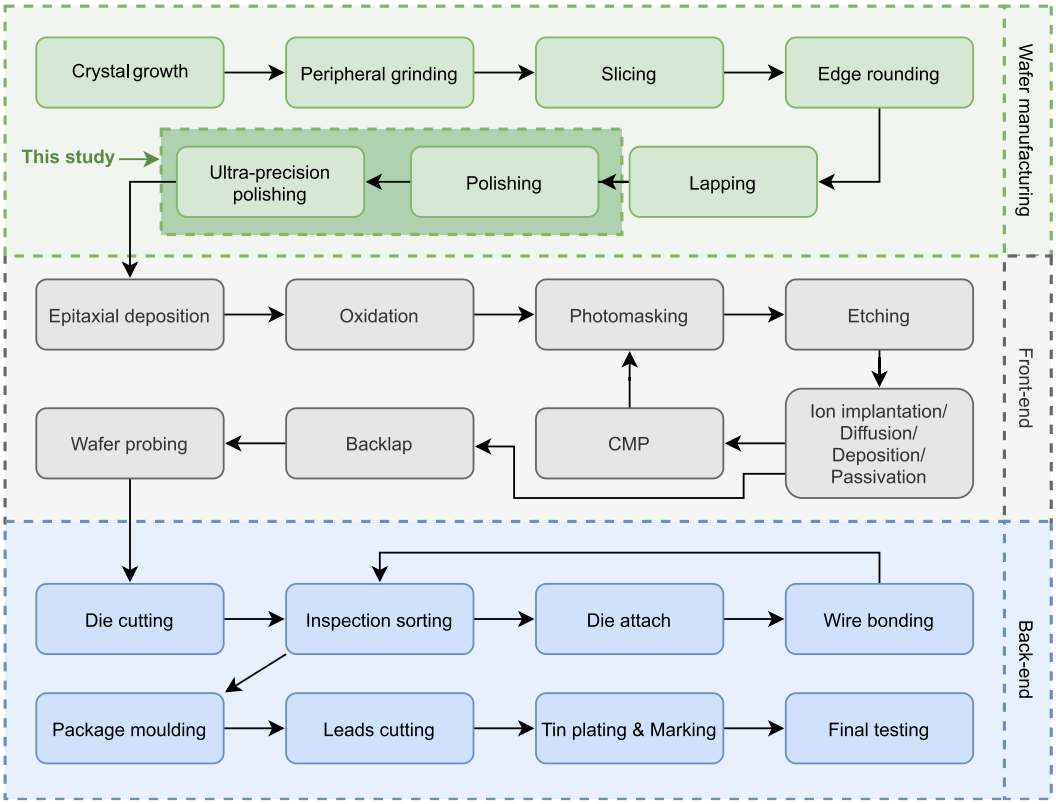


Figure 2.2 Semiconductor device fabrication process flow.

(1) Crystal growth. For silicon and many other crystal materials, Czochralski (CZ) method is used to fabricate the single crystal. In the CZ method, a small seed crystal is inserted into the melt of the substrate material, and the single crystal

is obtained by slowly pulling the seed upwards [23]. However, SiC will not melt but directly sublimate into vapour when heated, therefore, the CZ method is not applicable. To overcome this problem, the Lely method was invented in 1955, and its modified version became the dominant method for SiC growth [24]. In the modified Lely method, as shown in **Figure 2.3**, SiC source material (usually SiC powder) is heated and decomposed into sublimation of Si, Si_2C, and SiC_2 [25]. The pressure difference of the sublimation between the hot SiC source and the relatively cold SiC seed is the driving force for the modified Lely method. The SiC boule growth is governed by **Equation 2.1** [26].

$$\begin{aligned} SiC_2(gas) + Si(gas) &\leftrightarrow 2\,SiC(solid) \\ SiC_2(gas) &\leftrightarrow 2C(solid) + Si(gas) \\ SiC_2(gas) + 3Si(gas) &\leftrightarrow 2\,Si_2C(gas) \end{aligned} \tag{2.1}$$

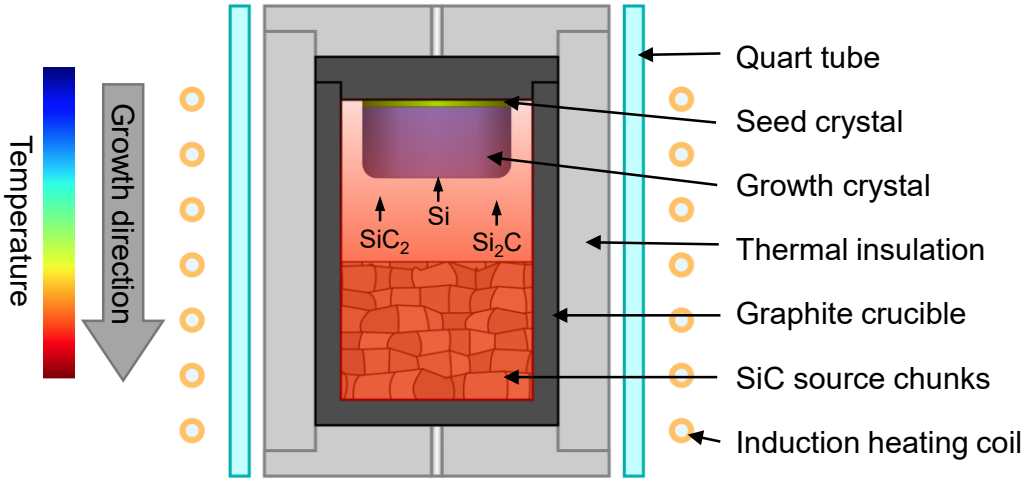


Figure 2.3 The schematic diagram of the modified Lely method.

(2) Peripheral Grinding. This process consists of three steps: crystal trimming, diameter grinding, and flat grinding. The crystal trimming is used to remove the excessive leftover material from the crystal growth, such as from the top and bottom of the boule. Diameter grinding controls the diameter of the boule to a standard size. An orientation flat or a notch is then added by flat grinding to indicate the crystal orientation. The original boule will be cut into standard blocks, as shown in **Figure 2.4**.

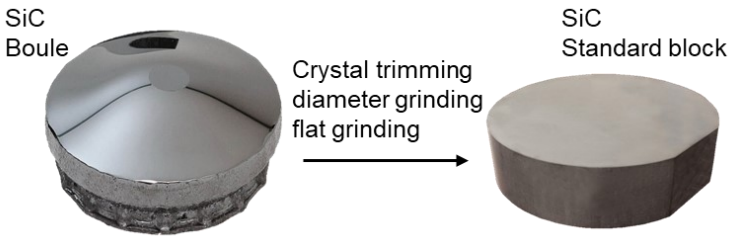


Figure 2.4 SiC before and after peripheral grinding [27].

(3) Slicing. This step slices the standard block into thin wafers with standard thickness. Wire-saw or rotating diamond inner peripheral blades are utilized depending on the diameter of the wafer [28].

(4) Edge rounding. After slicing, the edge of the wafer will be very sharp, which fractures easily and produces unacceptable scraps. Meanwhile, a sharp edge can also damage the polishing pad. A profiled diamond wheel is utilized during edge rounding to remove sharp and brittle edges. In addition, edge rounding can also adjust the final diameter of the wafer [28].

(5) Lapping. Lapping is used to removing the slicing striations and reduce the wafer-to-wafer thickness variation and total thickness variation (TTV) [29]. After slicing, the wafer-to-wafer thickness variation can be over 20 μm, and the TTV exceeds 5 μm. After lapping, the TTV drops below 1 μm, surface roughness Ra below 0.3 μm, and wafer-to-wafer thickness variation within a few micrometers. Dual-side lapping is generally used, and the thickness of the damaged layer can be reduced as well [28].

(6) Polishing. This step refers to the mechanical polishing of the lapped wafer to improve surface quality, reduce subsurface damage and residual stress layer. A double-side polishing machine is employed, and ultra-hard abrasives such as diamond are used to achieve high efficiency. The material removal rate of this step is several μm/h, and the resulting surface roughness is several nanometers.

(7) Ultra-precision polishing. This is the final step of processing wafers that will determine the final surface and subsurface quality. Ultra-precision polishing is

aimed to obtain a damage-free surface with sub-nanometer level roughness [30]. Many methods have been developed to achieve this goal, and currently, CMP is regarded as the best global planarization method with ultra-precision, which is also applied in the manufacturing of SiC wafers [31]. More discussion on ultra-precision polishing is given in the following section.

2.2 Ultra-precision polishing method

Substantial effort has been devoted to developing an ultra-precision polishing method to obtain an atomically flat and damage-free surface. The initial ultra-precision polishing method is based on the modification of mechanical polishing. Mechanical based surface finishing method such as grinding, lapping, and polishing has been widely used in industry. Conventional mechanical polishing contains both brittle fracture and ductile deformation. The brittle fracture characterized by chipping and cracking is the dominant material removal mechanism in conventional mechanical polishing, which leads to serious sub-surface damages and must be controlled in ultra-precision polishing [32]. The transition from brittle to ductile material removal is often observed at a small cutting depth. Bifano *et al.* find that ceramic materials exhibit a brittle-ductile transition at a critical depth of indentation d_c, as expressed in **Equation 2.2** [33]:

$$d_c = 0.15\left(\frac{E}{H}\right)\left(\frac{K_c}{H}\right)^2 \tag{2.2}$$

where E is the elastic modulus of the material, K_c is the fracture toughness, and H is the Vickers hardness. The material determines the coefficient, and the value 0.15 is valid for many ceramics, including SiC. The theoretical value of d_c of a 4H-SiC single crystal for the plastic–brittle transition is 20.8 to 64 nm as calculated by Chai *et al.* [34]. At a cutting depth smaller than d_c, the energy required to propagate a crack is larger than the energy required for plastic yielding, so ductile deformation will be dominant [33]. Hence, for mechanical-based ultra-precision polishing, a small cutting depth or small grain energy is needed. Nanogrinding and

Magnetorheological Finishing (MRF) are based on this mechanism to achieve a low roughness surface.

The mechanical-based removal can achieve a low roughness; however, the ductile mode removal mechanism is eventually employed to remove surface material, which also introduces an amorphous layer into the surface. It is impossible to confine the energy of each grain within the need to remove an atom, and the excessive force will always influence the subsurface. Thus, it is challenging for mechanical-based methods to achieve atomic precision. Meanwhile, a low cutting depth reduces the material removal rate. Hence, a chemical process has been introduced to provide a damage-free surface. The chemical modification can soften the surface and further decrease the mechanical energy needed to remove the surface material. In some circumstances, the chemical corrosion can directly remove material without introducing any damage. Chemical reactions can focus on the outermost layer of atoms and do not affect the atom beneath, thus have the potential to do atomic precision material removal.

In this section, the state-of-the-art ultra-precision polishing methods, including nanogrinding, magnetorheological Finishing (MRF), ion beam figuring (IBF), chemical mechanical polishing (CMP), elastic emission machining (EEM), tribochemical polishing (TCP), plasma assisted polishing (PAP) and catalyst-referred etching (CARE) will be introduced.

2.2.1 Nanogrinding

Nanogrinding can produce a surface with lower roughness and lower damage than conventional mechanical polishing. SiC with a surface roughness Ra of 0.42 nm and flatness less than 1.0 μm have been achieved by Huo *et al.* using a precision nanogrinding machine with fine diamond wheels as shown in **Figure 2.5** [35]. The #12000 diamond cup wheel with an infeed rate of 0.25 μm/min was used for the result, which is much higher than conventional mechanical polishing using

submicron size grain (~1 μm/h) [35]. In nanogrinding, ultra-precision machines with high motion accuracy and high stiffness are utilized to control the grinding wheel [36]. The cutting depth can be controlled down to the nanometer level. Since the cutting depth can be precisely controlled to be equal or less than the critical depth of ductile removal (*e.g.,* 20.8 to 64 nm for SiC), the brittle fracture can be restrained, and ductile deformation is the predominate material removal mechanism [37]. Surface roughness and SSD can thus be drastically reduced.

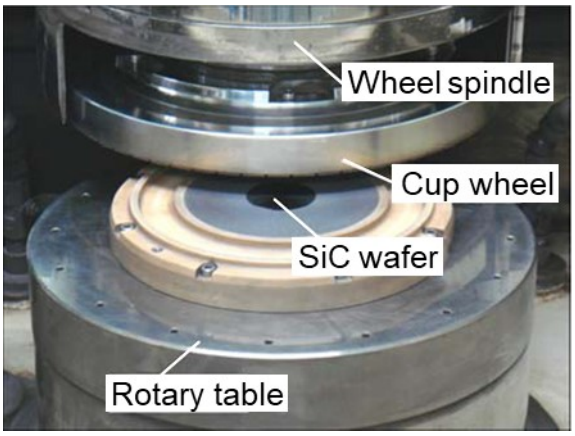


Figure 2.5 The optical photo of the nanogrinding setup [35].

The cutting depth of nanogrinding can be better controlled than mechanical polishing, which suffers from deep scratching from the randomly higher cutting depth of inevitable oversize grains. The oversized grains in mechanical polishing support a disproportionate load, and thus producing a much deeper cut and bringing brittle fractures extending into the wafer of several microns [35]. Nanogrinding uses a diamond cup wheel with a highly determinized cutting path of the individual grains, thus avoiding deep scratches and controlling the flatness. Nanogrinding has the potential to replace lapping and mechanical polishing. Although this method can suppress microcracks and achieve a relatively high material removal rate (MRR) of 0.25 μm/min and sub-nanometer roughness, The formation of amorphous layer and subsurface damage is inevitable due to the ductile deformation [38].

2.2.2 Magnetorheological Finishing (MRF)

MRF utilizes magnetorheological (MR) fluid to carry the polishing abrasives. It was invented by William *et al.* at the Luikov institute of heat and mass transfer in Minsk, Belarus, in the late 1980s [39]. The schematic diagram of MRF is shown in **Figure 2.6**. The carrier wheel contains an electromagnet or permanent magnet inside, which generates a magnetic field between the wheel and the workpiece. When the MR fluid is injected into the gap, the magnetic field will pull it against the wheel surface and form an MR fluid ribbon. The workpiece surface can be finished when in contact with the MR fluid ribbon due to normal and tangential cutting forces applied by the abrasives in the MR fluids [40]. Usually, MRF is a sub-aperture polishing tool. A sophisticated computer program is needed to control the workpiece sweep through the polishing zone.

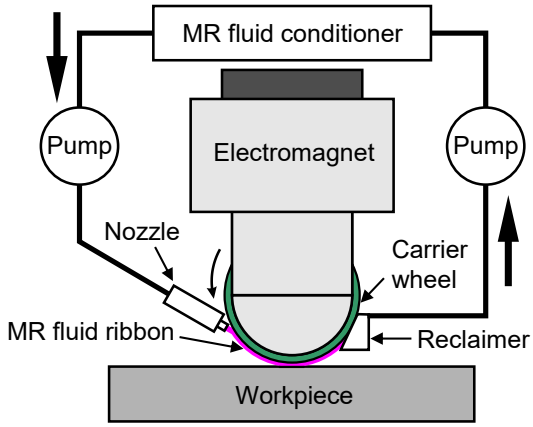


Figure 2.6 The schematic diagram of the MRF process.

The polishing mechanism of MRF is shown in **Figure 2.7**. When the MR fluid is delivered into the magnetic field, chains of magnetic particles will form and grip abrasive particles in between. The yield stress developed in the MR fluid can restrict the free movement of grains to some extent and drive them to interact with the workpiece with a larger shear force. This results in the removal of loosely held particles and shearing of peaks in the form of microchips and thus reduces the surface roughness [40, 41].

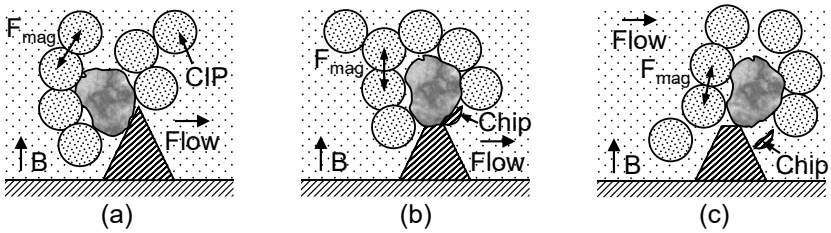


Figure 2.7 Finishing action in MR fluid. (a) Abrasive grain and CIP chains approach roughness peak; b) abrasive grain takes a small cut on roughness peak in the presence of bonding forces; c) material is removed in the form of microchip during cutting action [41].

During the MRF processing of SiC, the material removal rate can be very low since SiC has high hardness. Diamond abrasives are often employed to MRF polish of SiC. Cheng *et al*. reached a roughness of 1.14 nm on reaction-bonded silicon carbide (RB-SiC) after 50 hours of MRF using diamond powder as a nonmagnetic abrasive [42]. Pan *et al.* achieved an Ra of 1.9 nm on 6H-SiC via a cluster magnetorheological effect plane polishing machine [43]. Yin *et al.* suggested that the surface roughness of SiC wafer decreases with the size of diamond abrasives in the slurry [44]. Ultra-fine diamond abrasives are needed to achieve an atomically flat surface. However, the polishing efficiency and pressure drop dramatically due to the invalidation of the accommodation-sinking effect for ultra-fine abrasive and magnetic particles [45]. This could be the reason for the over 1 nm roughness limitation for the MRF of SiC using nano-diamond abrasives. To solve the problem, Chemical additives such as oxidants and catalysts are often added into the MR fluid to facilitate the modification of SiC to form a softer layer that can promote polishing efficiency. Deng *et al.* obtained a SiC surface with an Ra of 0.33 nm using MRF with H_2O_2 as the composite catalyst particles [46]. Liang *et al.* achieved an Sa of 0.4955 nm on single-crystal SiC using chemical magnetorheological finishing (CMRF) based on Fenton reaction [47]. Those results are far outpacing conventional MRF.

MRF and its derivative methods are capable of achieving an atomically smooth surface. However, the overall efficiency of MRF is still very low because it is a sub-aperture method. The general MRR of MRF is below 0.2 μm/min [42]. Meanwhile, contaminations such as Fe particles are often introduced into the sample [48]. Also,

the diamond particles used in processing SiC might introduce new damages.

2.2.3 Ion Beam Figuring (IBF)

IBF is a typical non-contact polishing technique based on ion beam sputtering. It can achieve ultra-precision finishing with sub-nanometer surface roughness. Meanwhile, IBF does not cause tool wear or edge effect due to its non-contact nature. **Figure 2.8** shows the schematic diagram of the IBF setup. Noble gases ions like Ar are generally used in IBF. During the operation, the Ar gas was delivered into the chamber in the ion beam source can be ignited into plasma by the RF power. The Ar^+ ions in the plasma accelerate and are focused onto the workpiece by the graphite grid system. A hot-cathode neutralizer adds electrons into the ion beam to prevent the charging effect. A smaller beam can be obtained by adding an aperture; the smallest available is 0.5 mm [49]. The material on the workpiece surface can be removed by the bombardment of accelerated Ar^+ ions.

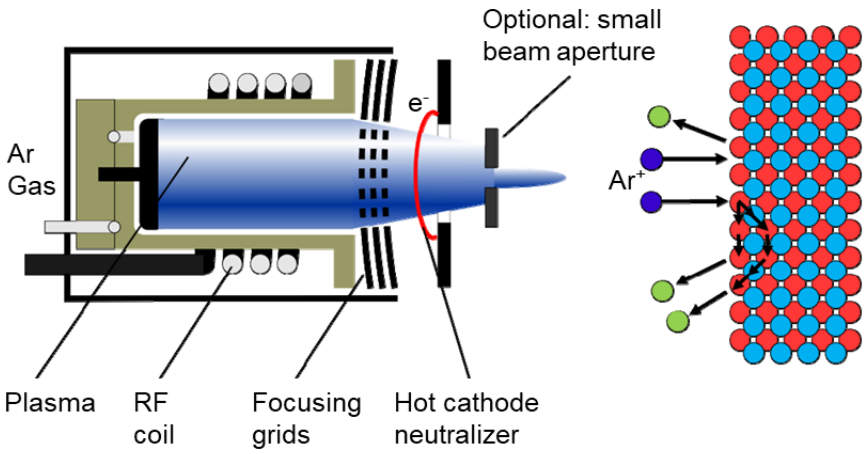


Figure 2.8 The schematic diagram of the IBF setup [49].

IBF has been widely used in precision optics like lithography, X-ray, and astronomical telescopes. Arnold *et al.* utilized IBF to reduce the Rq of SiC X-ray mirror to ~0.5 nm from the initial mechanical polished surface with Rq = 2.15 nm [50]. Weiser *et al.* reported an RMS of 0.13nm on a serial sphere for lithography optics after IBF [51]. Despite the high precision, IBF still faces many challenges. David concludes the challenge of IBF as process adjustment for a predictable

removal function, measurement challenges, and secondary effect [49]. Meanwhile, Carbon contamination is easily introduced from the graphite grids inside the ion source that accelerate and focus the ions beam [49]. In addition, the equipment for IBF is extremely expensive, and the material removal rate of IBF is particularly low (tens of nm/min only at the beam centre) [52]. Currently, IBF is only performed at the final step in high-end ultra-precision optical manufacturing and is not suitable for serial production.

2.2.4 Chemical Mechanical Polishing (CMP) and modified CMP

CMP was first invented by Beyer from IBM in 1983 and has now been widely used in the semiconductor industry for the planarization of wafers to avoid distortion during lithographic imaging [53]. CMP is a hybrid polishing process that uses chemical reactions to make the sample surface soft and then mechanical interaction to remove the modified surface material. The schematic diagram of the CMP setup is shown in **Figure 2.9**. A polishing pad made of polyurethane polymer is fastened on a round platen. The wafer is fastened on the wafer carrier and rotates in the same direction with the polishing pad. The chemicals in the slurry react with the wafer surface, forming a relatively soft modified layer. The modified layer is then removed by mechanical abrading. The hardness of the abrasive is generally similar or softer than the wafer substrate to prevent the direct removal of material from the wafer via mechanical effect, which could cause scratching [54].

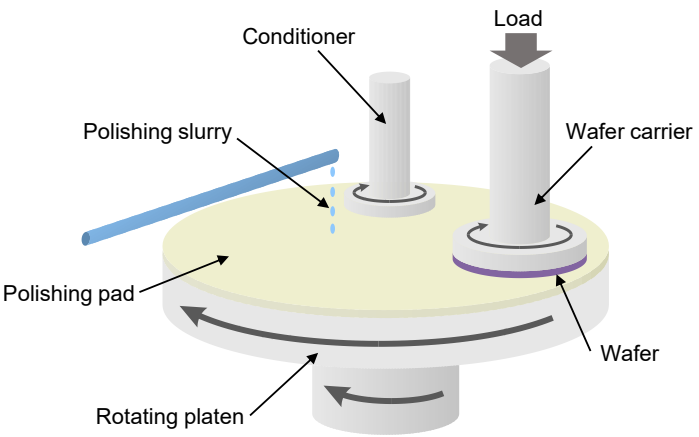


Figure 2.9 The schematic diagram of the CMP setup.

CMP has been widely applied in the high-precision polishing of SiC. Zhou *et al.* first used CMP to polish SiC; they achieved a damage-free surface with RMS of 0.5 nm using concentrated colloidal silica slurry at temperatures higher than 55°C and a pH value higher than 10 [55]. The chemical modification process of SiC CMP generally utilizes OH^- groups in the slurry to weaken the Si-C bonds and promote the oxidation of the SiC surface to form soft SiO_2. The widely used oxidants contain HF, H_2O_2, CrO_3^-, MnO_4^-, OCl^-, etc. [56, 57]. Pan *et al.* used H_2O_2 as the oxidant, KOH to provide OH^- and colloidal silica as the abrasive to polish SiC [58]. They obtained an atomically flat defect-free surface with atomic step-terrace structure and roughness of 0.0667 nm with a high MRR of 105 nm/h [58]. Zhou *et al.* used colloidal silica abrasive and Fe nanoparticles as the catalyst to provoke H_2O_2 to generate *OH hydroxyl radicals based on Fenton reaction [59]. The active *OH can induce the oxidation of SiC, an MRR of 120 nm/h has been achieved, and a roughness Ra of 0.05 nm has been observed on the entire surface. Chen *et al.* obtained a maximum MRR (1089 nm/h) of SiC with an average roughness Ra of 0.11 nm using colloidal ceria-based slurry in a strong acidic (PH = 2) $KMnO_4$ environment [60]. $KMnO_4$ serves as a strong oxidizer of the SiC surface; the oxidized species of SiC (e.g., $Si_xC_yO_z$ or SiO_xC_y) could be further oxidized or hydrolyzed to form carbon-free silicon oxide species and can be quickly removed by mechanical abrasion [61]. Hoshino *et al.* found that ceria has the chemical tooth property and can form Si-O-Ce bonds during the CMP of SiC, which can be rapidly removed by mechanical abrasion force and further promote the MRR [62].

CMP is an efficient method to obtain a defect-free and ultrasmooth surface. However, it is difficult to achieve both high MRR and low surface roughness SiC due to the high hardness and high chemical inertness. To overcome the limits, many methods have been utilized to promote the chemical modification of the surface. Electrochemical mechanical polishing (ECMP), photocatalytic-assisted chemical mechanical polishing (PCMP), ultrasonic-assisted chemical mechanical polishing (UCMP), and laser-assisted chemical mechanical polishing (LCMP) will be briefly

introduced in the following paragraphs.

ECMP combines anodic oxidation with a typical CMP technique: anodizing SiC to form an oxidized layer and then removing the oxidized layer via mechanical abrasion. Li *et al.* first applied ECMP on SiC and obtained a final Ra of 0.2 nm with an anodic current of 1mA/cm^2 [63]. Deng *et al.* observed a significant hardness reduction of the SiC surface from 34.5 GPa to 1.9 GPa due to the formation of an anodized layer; they achieved a Ra of 0.23 nm and MRR of 0.42 μm/h on 4H-SiC using ECMP with CeO_2 slurry [64]. Murata *et al.* utilized ECMP with polyurethane–CeO_2 core-shell particles as abrasive and achieved a high MRR of 3.82 μm/h; the resulting surface has a Ra of 0.5 nm [65]. For ECMP of SiC, fast anodization is needed to obtain a high MRR. However, faster anodization will form a porous surface due to unevenly anodization, restricting ECMP from achieving an atomically smooth surface at high speed [63].

PCMP uses photocatalysts to absorb light energy to dissociate H_2O into *OH radical. The active *OH radicals then react with SiC and form SiO_2, then the SiO_2 is removed by CMP. Zhou *et al.* added a photocatalyst incorporated pad and a UV light system in typical CMP; the pad employs the photocatalytic effect of TiO_2 to increase the *OH concentration [66]. The MRR of 4H-SiC has been increased to 200 nm/h with a Ra of 0.0539 nm [66]. Yan *et al.* studied the influence of PCMP parameters and found that the greater the rate of UV photocatalysis reaction, the greater the MRR of the 6H-SiC wafer and the lower the final surface roughness Ra [67]. They achieve a Ra of 0.423 nm with an MRR of 107 nm/h under optimized conditions. Yuan *et al.* performed PCMP with TiO_2 as the photocatalysis, H_2O_2 as the electron capturer, SiO_2 as the abrasive, and $(NaPO_3)_6$ as the dispersant, and obtained the highest MRR of 0.95 μm/h and the best surface finish (Ra = 0.35 nm) [68]. The development of PCMP is mainly restricted by the efficiency of the photocatalytic reaction.

UCMP utilizes ultrasonic vibration to drive additional effective abrasive

particles to increase polishing efficiency. Liu *et al.* claimed that ultrasonic elliptical vibration could effectively improve the MRR while maintaining surface quality in conventional CMP; they achieved a high MRR of 693.6 nm/min on Si wafer, while the Ra was only 10.61 nm [69]. Hu *et al.* combined UCMP with ultrasonic lapping and achieved the highest MRR of 1.057 μm/h and the lowest PV of 0.474 μm. They suggested that ultrasonic could contribute to driving the chemical corroding of SiC in CMP slurry and forming Si-C-O and Si-O bonds [70]. Yang *et al.* combined ultrasonic with ECMP and confirmed that ultrasonic vibration could significantly enhance the anodic oxidation of SiC [71]. Ultrasonic can boost the MRR of CMP SiC; however, no report of UCMP SiC to atomic flatness can be found, which might be due to ultrasonics increasing the impact of abrasives, making it hard to achieve atomic precision [70].

LCMP employed a nanosecond laser or femtosecond laser to modify the surface during CMP. For nanosecond laser, the strong thermal effects can melt the surface material, vapourize or decompose chemically, and easy to form a deposited layer [72]. The modulated layer can be tens of micron thick for nanosecond laser; thus, it is unsuitable for ultra-precision polishing [73]. The thermal effect of the femtosecond laser is much smaller due to its short pulse duration and high pulse frequency and is widely used in material processing to improve surface quality [74]. Wang *et al.* achieved an MRR of 979.8 nm/h with a Ra of 17 nm on the 4H-SiC [75]. The femtosecond laser can induce an SSD layer of 1-2 μm due to the subsurface inhomogeneous laser ablation, which cannot meet the needs of damage-free material removal [76]. LCMP can achieve high MRR, but the roughness is over ten nanometers and far from the atomic level.

CMP is the most commonly used global planarization method capable of achieving an atomically smooth surface. However, CMP is time-consuming as the MRRs of SiC and other chemically inert materials are very low. Many derivative methods that employ novel modification mechanisms have been investigated to

solve the problem, as discussed before. The improvement of MRR is often accompanied by the deterioration of surface quality; sub-nanometer level surface roughness is hard to obtain for the method with the highest MRR. Great promotion of the chemical modification process could lead to excessive etching and forming corrosion defects [77]. Overall, the modified CMP methods can increase the MRR for achieving sub-nanometer roughness surface to ~ 1 μm/h. In addition, CMP and its derivative methods need to frequently replace the consumables such as abrasives, chemical slurries, and polishing pads, which further escalate the maintenance cost [78]. Besides, some of the slurries could seriously pollute the environment.

2.2.5 Elastic emission machining (EEM)

EEM is one of the most precise finishing methods that can remove material at the atomic level [79]. It has been applied in fabricating extremely precise surfaces such as extreme ultraviolet (EUV) lithography and X-ray microscopy. EEM is a non-contact method that utilizes the surface chemical activity of water-suspended ultra-fine powders. The schematic diagram of EEM is shown in **Figure 2.10**, where a rotating tool and workpiece are immersed in a slurry. The rotating tool is made of soft material such as polyurethane rubber, while the slurry contains water and very fine abrasive particles such as SiO_2, Al_2O_3, and ZrO_2. The rotating tool is not in direct contact with the workpiece, and the gap between the tool and workpiece is filled up by a thin lubrication film of fine abrasive slurry due to the hydrodynamic effect [80]. The collision between ultra-fine particles and the workpiece will induce chemical reactions that remove the surface atoms out of the workpiece. As the binding energy of the topmost layer of the workpiece is smaller than the adjacent layer, it is possible to remove the topmost layer of atoms without affecting the subsurface [81].

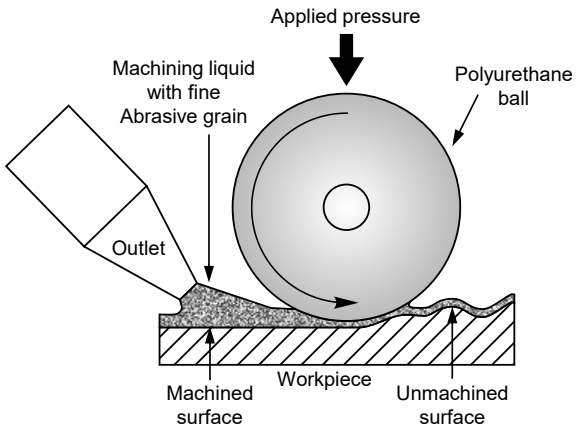


Figure 2.10 The schematic diagram of the EEM setup [80].

Kubota *et al.* reported that the SSD and scratches on 4H-SiC can be completely removed by EEM, and the processed surface is atomically flat [82]. They obtained a damage-free surface with RMS roughness of 0.1 nm and MRR of 20 nm/h, and the PSD analysis revealed that the surface is smoothed in the spatial wavelength range below 10 μm [83]. EEM can produce atomic level surface without stress; however, the MRR of EEM is extremely low. Hence EEM can only be applied at the final step of finishing in manufacturing of high-end ultra-precision optics currently, similar to IBF.

2.2.6 Tribochemical polishing (TCP)

TCP is an abrasive-free polishing method that utilizes the tribochemical reaction between the polishing plate and workpiece to dissolve the material from the workpiece surface [84]. Zhu *et al*. first applied TCP on polycrystalline silicon carbide, and they compared the influence of oxidant solution (including CrO_3, H_2O_2, and $KNnO_4$) to the polishing of polycrystalline SiC [56]. A surface roughness below 1 nm and MRR of 0.2-0.4 μm/h had been obtained using Si_3N_4 polishing plate and 3 wt.% CrO_3 oxidant solution. Kubota *et al.* utilized a soda-lime SiO_2 glass plate to TCP 4H-SiC and achieved a low roughness of RMS 0.1 nm with a high MRR of 0.775 μm/h [85]. They attributed the high MRR to the high hardness particles, higher water adsorption ability, and higher frictional heat of the soda-lime SiO_2 glass plate.

2.2.7 Plasma assisted polishing (PAP)

The fundamental mechanism of PAP is very similar to CMP, where the plasma is used to modify the SiC surface to form a soft modified layer, and then the modified layer is removed by mechanical abrasion. PAP was proposed by Yamamura *et al*. from Osaka university; the schematic diagram of the PAP setup is shown in **Figure 2.11** [86]. The PAP setup consists of a plasma generator and a mechanical removal part. A typical 13.56 MHz power source was applied to generate atmospheric pressure plasma from helium-based water vapour. The mechanical removal part applies a polishing film placed at the tip of a spindle. Moreover, the wafer was mounted on a rotary table. The water vapour plasma containing a high concentration of *OH radicals was used for surface modification during PAP. SiC substrate irradiated by water vapour plasma was oxidized by *OH radicals, forming softer products such as SiO_2 and silicon oxycarbide transition layer on the surface. The hardness of the SiC surface has been reduced from 37.4 ± 0.5 GPa to 4.5 ± 0.8 GPa by the plasma modification of the surface composition, XPS confirms the formation of Si–O and Si-C-O bonds, and a roughness RMS of 0.14 nm was obtained [87]. Deng *et al.* studied the influence of the abrasive and found CeO_2 is better in preventing scratches than Al_2O_3 abrasive [88]. The abrasive should be softer than the workpiece to prevent scratches or SSD. Deng *et al.* also proposed that the MRR of PAP depends on the oxidation rate, and they achieved a Ra of 0.06 nm with an MRR higher than 185 nm/h [88-90]. PAP has also been proved efficient in polishing difficult-to-machine materials, including GaN, AlN, sapphire, and Diamond [91-94]. PAP can obtain an atomically flat surface without introducing SSD. Meanwhile, it is a dry process that does not consume slurry and polishing pad, which can reduce the maintenance cost. The main factor that limits the application of PAP on SiC is the low MRR originating from a low oxidation rate.

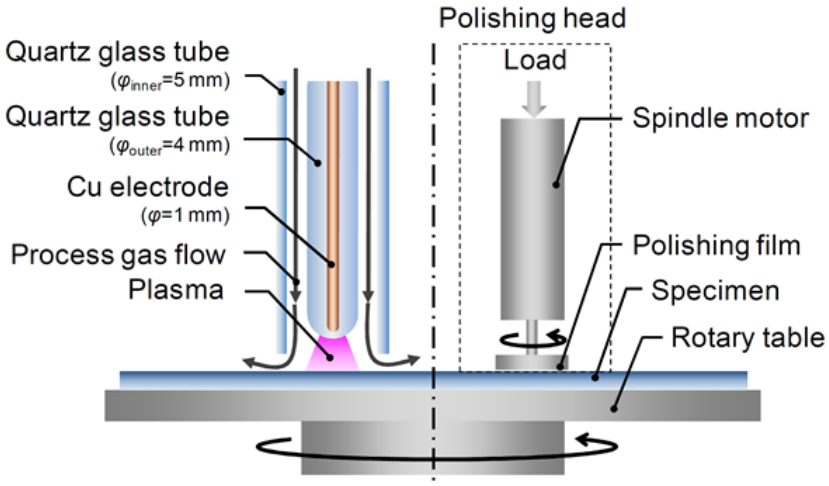


Figure 2.11 The schematic diagram of the PAP setup [86].

2.2.8 Catalyst-referred etching (CARE)

Catalyst-referred etching (CARE) was proposed by Hara *et al.* from Osaka University in 2006 [95]. The mechanism of CARE is shown in **Figure 2.12**. A polish plate made of Pt is used as the catalyst, and HF is used as the etchant. During operation, chemical etching occurs only near the surface of the catalyst plate, which also serves as a reference during the flattening of substrate [96]. The Pt serves as a catalyst that removes the valence electrons from the contacting area on the SiC surface and preferentially oxidizes those locations. In the meantime, the oxide product is etched by the HF etchant [97]. Hara *et al*. obtained a smooth SiC surface with a Ra of 0.089 nm; the atomic step-terrace can be observed clearly [95]. Okamoto *et al.* measured the MRR of CARE SiC and found a strong correlation between the MRR and atomic-step density on 4H-SiC; they obtained an MRR of 60 nm/h on 8° off-axis substrate while only 1 nm/h on on-axis sample [96]. The result shows that CARE can obtain a damage-free surface with atomic surface roughness; however, the low MRR limits its application for serial production.

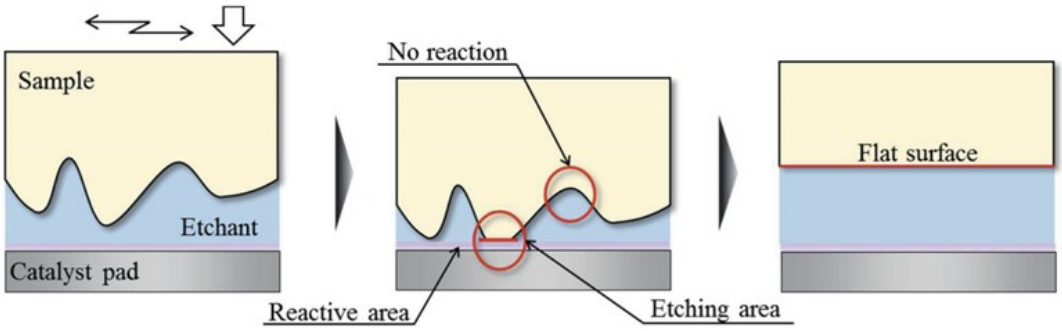


Figure 2.12 The schematic diagram of the mechanism of CARE [98].

2.3 Truly-atomically flat surface fabrication

The development of manufacturing technology has always been chasing higher precision. Fang concludes the next phase of manufacturing as atomic and close-to-atomic scale manufacturing (ACSM), where the material removal, transformation, and addition are at atomic precision [2]. One of the essential fields of ACSM is the manufacturing of truly-atomically flat surfaces. It is also known as the roughness limit of a surface in applied physics [13]. The current ultra-precision polishing method can provide atomic-level roughness; however, the surface is not perfectly atomic flat. **Figure 2.13(a)** shows a schematic diagram of the typical CMP surface. The surface consists of periodic atomic steps. The atomic steps are originated from the small off-angles from slicing, which is inevitable since the slicing cannot be perfectly parallel to a crystal facet even for on-axis substrate.

Ideally, the highest precision for manufacturing a surface is truly-atomically flatness, which implies that all the topmost surface atoms are in a single layer of crystal facet (as shown in **Figure 2.13(b)**). Truly-atomically flat surface has superb properties and can promote intrinsic material properties, quantum device fabrication, surface reaction mechanism, and atomic friction [99-101]. Methods that can achieve that standard are rare and have ultralow efficiency and manufacturing scale at present. The typical method including exfoliation, thermal annealing, chemical etching, and atom manipulation will be introduced.

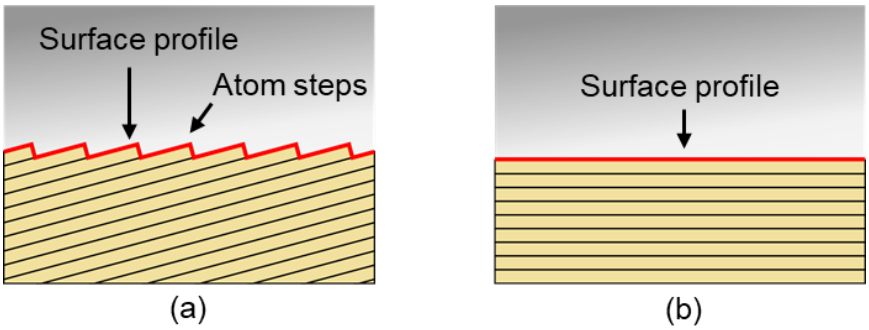


Figure 2.13 The schematic diagram of (a) typical CMP surface with atomic flatness and (b) truly-atomically flat surface.

2.3.1 Exfoliation

Exfoliation methods are widely used for the exploration of emergent 2D materials. The first graphene is prepared using mechanical exfoliation, and the investigation of many intrinsic properties, such as quantum Hall effect and superconductivity, are explored based on the sample from the mechanical exfoliation method [99, 102, 103]. Mechanical exfoliation is generally applied on layered hybrid type crystal, where 2D sheets are stacked in layered order by van der Waals force. By overcoming the van der Waals attraction between the 2D sheets by mechanical force, a single-atom layer with a truly-atomically flat surface can be obtained. The mechanical action can be applied using normal force or lateral force, and the actual operational methods contain micromechanical cleavage, sonication, ball milling, fluid dynamics, detonation, supercritical fluid exfoliation, etc. [104].

More recently, ion-intercalation, liquid exfoliation, electrochemically-assisted exfoliation, and Au-assisted exfoliation methods have greatly improved the usability of this method [105-108]. For instance, the Au-assisted mechanical exfoliation proposed by Huang *et al.* utilizes the higher interaction energy to Au than the interlayer energy of most layered crystals; they demonstrated a successful exfoliation of 2D sheets from 40 layered materials [108]. The exfoliation method is relatively easy to operate and can produce a high-quality surface. However, the exfoliation method can only operate on layered material, greatly restricting its

application. Meanwhile, it is still limited in lateral size, yield, and unexpected contaminations.

2.3.2 Thermal annealing

Thermal annealing of Si wafer in ultrahigh vacuum (UHV) or argon and hydrogen ambient can produce an atomically flat surface [109, 110]. The surface is cleaned by thermal cracking during thermal annealing and reconstructed by surface diffusion and atomic dimerization [109]. The rearranging of surface atoms during annealing can smooth the surface and release internal stress [111]. Thermal annealing is also used to prepare the atomically flat subtract for advanced applications like quantum devices [100]. Thermal annealing can produce high-quality surfaces for bulk materials and is suitable for serial production. However, thermal annealing often spontaneously form atom structures since the generation of extra steps could decrease the total surface energy in certain circumstances [109].

2.3.3 Chemical etching

Pure chemical etching sometimes can produce a near-atomic flat surface. For instance, aqueous KOH solution etching can be used in micromachining of Si to provide an essentially perfect and atomically flat surface owing to its selective etching of all Si surfaces except Si(111) surface [112]. Using NH_4F etchant, near-atomically flatness can also be obtained on Si(100) surface [101]. For SiC, hydrogen etching at high temperatures is an ordinary operation to eliminate scratches and obtain a clear atom step surface [113]. However, the highly site-specific etching will result in inhomogeneities in the etchant that will severely affect the etching of the surface [114]. Meanwhile, chemical etching will preferentially attack the dislocation sites on a single crystal and form etching pits, damaging the surface integrity [115].

2.3.4 Atom manipulation

The most controllable method which can achieve ideal atomic precision is atom manipulation. Using tip-based methods like STM or AFM, researchers can accurately manipulate a single atom [116, 117]. The tip-based atom manipulation process can be divided into three steps: (i) Extraction of individual surface atoms to the tip. (ii) Relocation of the tip-atom combination. (iii) Release the atom from the tip to form atomistic construction. Atoms can be extracted by tip-sample contact (controlled tip crash), perturbation of metallic clusters, and inelastic electron tunnelling for breaking molecular bonds [116]. To manipulate atoms, the force applied by the tip needs to overcome the surface retaining force. The relocation of an atom requires sub-atomic precision. However, the released atoms are often preferentially absorbed by specific sites, such as the surface hollow sites or top surface atom sites on fcc (1 1 1) metal surface, which will restrict the design of atomistic construction [116]. The removal of single-atom layer precision with a relatively large (micron-level) area has been achieved by the AFM-based method [118]. It is theoretically possible to produce a truly-atomically flat surface by manipulating individual atoms. However, the manufacturing scale for atom manipulation is still too small. Associated with the ultralow efficiency, high demand for expensive equipment, and highly skilled operators, the application of atom manipulation is limited.

2.4 Proposal of plasma-based atom selective etching (PASE)

Ultra-high precision polishing of SiC for industrial application can be realized by the method present in **Section 2.2**. The summary is presented in **Table 2**, with data extracted from the mentioned publication and reasonable estimations when there is no directly available data. Most of the methods can meet the requirement of sub 0.1 nm roughness, which is about the limitation of polishing. Their common problem is a very low MRR on SiC due to the high hardness and chemical inertness of SiC.

For the second motivation, a truly-atomically flat surface can be fabricated by exfoliation, thermal annealing, chemical etching, and atom manipulation, as described in **Section 2.3**. Those methods were also plagued by low efficiency, and producing large area near-perfect surface is infeasible. A Novel method with high MRR and potential to produce a large-area truly-atomically flat surface without introducing any damage is needed.

Table 2 Overview of ultra-precision polishing methods (reasonable estimates are given for not directly available data).

Method	**Roughness (nm)**	**MRR (nm/h)**	**Reference**	**Drawbacks**
Nanogrinding	0.42 2.58 18.37	15000 60000 120000	[35]	Surface and sub-surface damage like scratches and amorphous layers.
MRF	0.33 0.4955 1.14	635.621 1850 9000	[46] [47] [42]	Overall MRR is low due to the sub-aperture nature; hard abrasive like a diamond is needed to increase MRR, introducing surface damage and contamination such as Fe particles.
IBF	0.5~3	2400~9600	[52]	Low MRR, need a high vacuum, expensive equipment.
CMP	0.05 0.0667 0.11	120 105 1089	[59] [58] [60]	Low MRR, consume expensive slurry and polishing pad, environmental pollution, mechanical stress, corrosion when using aggressive chemical.
ECMP	0.23 0.5	420 3820	[64] [65]	
PCMP	0.0539 0.35 0.423	200 950 107	[66] [68] [67]	
UCMP	20.2	1057	[70]	
LCMP	17	979.8	[75]	
EEM	0.1	20	[83]	Low MRR, requires high precision and expensive equipment.
TCP	0.1 <1	775 200~400	[85] [56]	Low MRR, mechanical stress.
PAP	0.05~0.15	185	[90]	Low MRR, contact method might have stress.
CARE	0.045 <0.1 <0.1 0.1	190 (4°) 1 (On-axis) 37 (4°) 500 (8°)	[119] [120]	Low MRR, toxic etchant (HF), and expensive catalysis plate (Pt)
PCVM	1~100	6000~6000000	[121]	Low surface quality

High MRR can be achieved by either increased mechanical force or chemical

corrosion. The mechanical manner is excluded since it could not meet the requirement of a near-perfect surface. Hence, the only solution is to find a highly reactive method. Atmospheric pressure (AP) plasma can fit the requirement as its highly reactive, contactless, and can operate in dry ambient. AP-plasma-based polishing methods have been studied for several decades, and many have shown ultrahigh MRR.

Plasma chemical vapourization machining (PCVM) is the first machining and polishing method based on AP-plasma. It was proposed by Mori *et al.* from Osaka University in 1993 [122]. They utilized a rotary electrode and 150 MHz radiofrequency (RF) power to generate plasma and achieved a high MRR of 6.4 μm/min on polysilicon carbide [121]. Sano *et al*. used PCVM to polish 4H-SiC; they achieved an ultrahigh MRR of 134 μm/min and 180 μm/min on the Si-face and C-face 4H-SiC, respectively [123]. However, the polishing effect only appears on the C-face, and the roughness increases in Si-face. Plasma jet machining (PJM) was developed by IOM (Leibniz Institute of Surface Modification) during the late 1990s, utilizing an RF-power (f = 13.56 MHz) or 2.45 GHz microwave-driven plasma jet source. PJM has achieved an MRR of 7.84 mm^3/h on sintered SiC with RF-power; however, the roughness can only be decreased to ~100 nm [124]. Reactive Atom Plasma Technology (RAPT) was developed by RAPT Inc (US) and Cranfield University in 2002 for optical finishing [125]. They used an inductively coupled plasma (ICP) source and fluoride-containing gas (NF_3, CF_4) as the reactive precursor. Subrahmanyan *et al.* observed an increase in roughness of SiC during RAPT, and they attributed it to the increased surface energy at damage sites and contrast in etch rate at grain boundaries [126]. Wang *et al.* from the Harbin Institute of technology developed atmospheric pressure plasma polishing (APPP) in 2006, utilizing capacitively coupled plasma (CCP) jet driven by 13.56 MHz RF power [127]. They obtained sub-nanometer roughness on the SiC surface, but MRR is very low. To increase MRR, Wang *et al.* employed ICP (f = 27.12 MHz) source for APPP and achieved a high MRR of 6 μm/min on SiC; however, a porous morphology

appears after ICP-APPP, and the roughness deteriorated [128]. More recently, Shi *et al.* from the National University of Defense Technology proposed arc-enhanced plasma machining (AEPM) in 2014, using arc-enhanced ICP (f = 27.12 MHz) source [129]. They obtained MRR of over 17 μm/min (0.55 mm^3/min) on SiC, nevertheless, deterioration of surface roughness also appeared in their study.

AP-plasma, especially ICP based plasma etching, is highly reactive and capable of providing an ultrahigh MRR on SiC. The surface roughness deterioration after ICP is the main problem that restricts its polishing performance. To solve the aforementioned problem, providing a large-scale truly-atomically flat surface fabrication method, and advance the limitations of polishing technologies, the plasma-based atom-selective etching (PASE) method is proposed.

The aforementioned plasma-based polishing methods are based on the isotropic etching polishing (IEP) mechanism. The etching process transforms a rough surface into a relatively flat morphological intersection of spherical surfaces. With the increase of the spherical radius, the surface becomes flat. However, the thermal fluctuation always leads to new etching sites, creating a spherical surface with a small radius, limiting the roughness reduction of the plasma-based polishing method. Researchers in this field are also using low-temperature plasma (CCP) or adding a cooling nozzle to cool down high-temperature plasma (ICP), however, the results were not satisfactory due to the highly reactive nature of plasma. Meanwhile, reducing temperature will significantly decrease the material removal rate of the etching process. Unlike most plasma-based methods, generating isotropic etchings at low temperature, and having relatively weak flattening ability, PASE is an anisotropic process that operates at high temperatures. PASE is based on selective removal of the atoms which constituted the surface roughness; this is also the most direct way to reduce roughness without influencing the subsurface material. As shown in **Figure 2.14(a)**, the rough surface of single-crystal 4H-SiC is formed by many atom steps. The chemical activity of the atom on the step-edge (SE-atom) and the step terrace (ST-atom) is different [130, 131]. Using the appropriate condition,

the etching speed of SE-atom can be much larger than that of ST-atom, and thus etching can expand along the step-edge, as shown in **Figure 2.14(b)**. When selective atom etching is applied on all the SE-atom of the surface, the SE-atoms can be quickly removed. As shown in **Figure 2.14(c)**, the atoms which consist of surface roughness could be removed, and the surface becomes truly-atomically flat.

PASE features ultra-high MRR and is theoretically able to reach the limit of roughness: truly-atomically flatness. The ultra-high MRR enables ultra-fast polishing speed. Unlike other ultraprecision polishing methods that could only start with a raw sample of nanometer roughness, this work only took 5 mins to directly polish a sliced 4H-SiC chip from the roughness of ~100 nm to ~0.05 nm, otherwise might take over 8 hours with the traditional polishing. Compared to exfoliation, thermal annealing, chemical etching, and tip-based method, which can only generate micron level truly-atomically flat surface, PASE can produce centimeter-level surface.

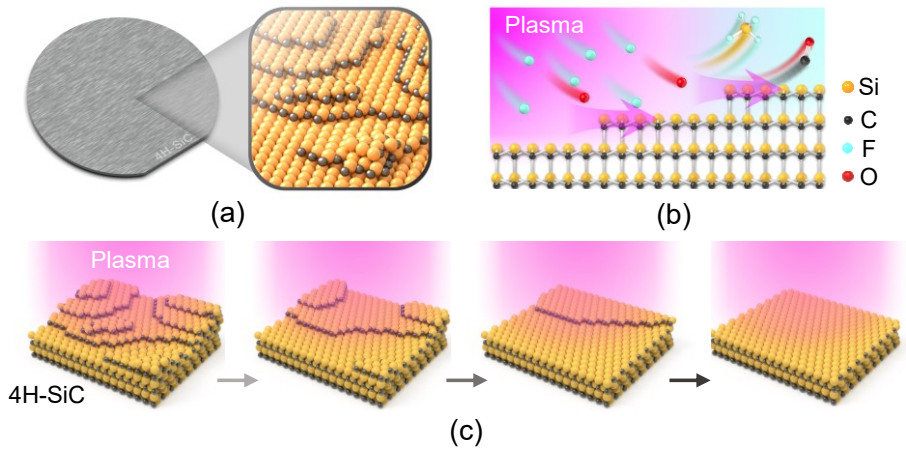


Figure 2.14 The schematic diagram of (a) Rough 4H-SiC surface, (b) PASE of atom steps, and (c) the polishing effect of PASE.

The lateral etching can remove the roughness layer without introducing any new subsurface damage; thus, this method is most effective and quickly reduces surface roughness. Meanwhile, the selectivity of this method is of atomic level; theoretically, when all atom-steps have been etched, the whole surface becomes truly-atomically flat with an integral crystal plane. Thus, this method could reach

the limitation of polishing. All single crystal material can be regarded as consisting of many atomic layers; hence, PASE can be applied as a general single crystal material polishing method. In this thesis, the polishing of SiC, Al_2O_3, GaN, AlN, and Si has been demonstrated [132]. The polishing speeds are all far outpacing the traditional CMP method. PASE could be easily applied on large-scale samples if a broad-scale evenly distributed plasma environment could be produced. The polishing time for 4H-SiC could be reduced from over 8 hours to 5 mins, reducing 12% of the total cost of wafer manufacturing [133]. PASE can significantly increase the polishing efficiency of many difficult-to-machine single crystal materials and facilitate third-generation semiconductor material application. Meanwhile, it advances the limitation of polishing technique and allows the future potential application of large-scale truly-atomically flat surfaces.

2.5 Summary

The state-of-the-art methods have been reviewed for solutions to the efficient polishing of 4H-SiC, and a potential approach to truly-atomically flat surfaces has been provided. Following that, PASE has been proposed.

(1) The background of WBG material, especially 4H-SiC, has been introduced. The whole wafer manufacturing process has been introduced to clarify the status of ultra-precision polishing of semiconductors, which is the main focus of this research.

(2) The state-of-the-art ultra-precision methods have been reviewed, the available methods for the fabrication of near-perfect surfaces have been presented. The merits and demerits of those methods have been summarized. Furthermore, the conclusion is that a highly reactive method is demanded for high MRR.

(3) To achieve highly reactive etching, AP-plasma has been introduced. The current AP-plasma-based method, including PCVM, PJM, RAPT, APPP, and AEPM, has been presented. AP-plasma, especially ICP based plasma etching, can

achieve high MRR. However, the surface roughness often deteriorates after etching.

(4) Based on AP-plasma, the PASE method has been proposed. PASE retains the advantage of high MRR by AP-plasma etching. Unlike other AP-plasma-based methods, which have relatively low precision due to isotropic etching, the polishing mechanism of PASE is based on selective removal of atoms that form roughness and has a precision toward an atom level. It can be a potential solution to fabricating a large-area near-perfect surface. The mechanism of PASE confines that it can only be conducted on single-crystal materials, meanwhile, it also implies that PASE could be applied as a universal single-crystal material polishing method.

Chapter 3

Apparatus development

3.1 Introduction

An appropriate plasma source is needed to realize PASE experimentally. Low-pressure plasma can often introduce damages due to ion bombardment, which must be prevented for damage-free polishing. Thus, AP-plasma has been chosen in this study. AP-plasma operates under high pressure; the mean free path becomes very low that it will not induce any damage by the bombardment effect. Temperature is another effect that must be considered in a chemical reaction. Here, CCP and ICP have been employed as plasma sources, representing low-temperature and high-temperature plasma, respectively. The molten KOH etching equipment has also been developed to test the etching effect in liquid phase chemical etchant rather than plasma.

In this chapter, the fundamental of CCP and ICP will be introduced. Two types of CCP, including direct and remote types, have been developed. Optimization of electrode material and cooling system will be introduced. For ICP, the improvement on ICP torch, sample holder, and environmental control strategies will be presented. To realize PASE in wet etching conditions, molten KOH etching has been employed. The conventional KOH etching system and its modification: the ultra-high temperature molten KOH etching system will be introduced.

3.2 Capacitively coupled plasma jet

3.2.1 Basic principles

CCP is widely used in the semiconductor industry for etching and deposition. The basic structure of CCP is shown in **Figure 3.1**, where two metal electrodes are separated by a small gap, forming a capacitor-type structure. One of the electrodes is connected to a radio frequency (RF) power supply (typically 13.56 MHz); the other is grounded. An RF electric field between the electrodes excites the gas in the gap into plasma through the electron avalanche effect.

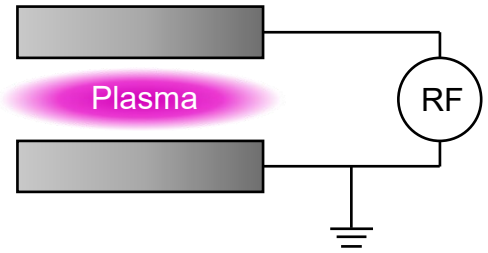


Figure 3.1 The schematic diagram of CCP.

Breakdown voltage can describe the difficulty of turning a gas into plasma. The breakdown voltage for a specific gas can be determined by Paschen's law:

$$V = \frac{Bpd}{ln(Apd) - ln(1 + \frac{1}{\gamma})} \tag{3.1}$$

where V is the gas breakdown voltage; A is the saturation ionization in the gas at a specific electric field/pressure; B is related to the excitation and ionization energies, both A and B are constants which can be determined experimentally; p is the gas pressure; d is the electrode gap distance, and γ is the secondary electron emission coefficient. From **Equation 3.1**, the breakdown voltage is related to the product of gas pressure times electrode distance. Thus, smaller gas pressure and electrode distance will lead to smaller breakdown voltage, making it easier to generate plasma.

The practical plasma etching system is shown in **Figure 3.2**. The plasma etching device is installed inside an enclosed metal chamber with an

electromagnetic interference shielded window and connected to a ventilation system to prevent possible health damage from electromagnetic radiation and toxic exhaust. Most equipment, including the mass-flow controller (MFC), the RF power supply (13.56 MHz), the matcher, and the 3-axis platform, are commercially available products. This study mainly requires the design of the plasma jet nozzle and the sample holder (in the case of ICP).

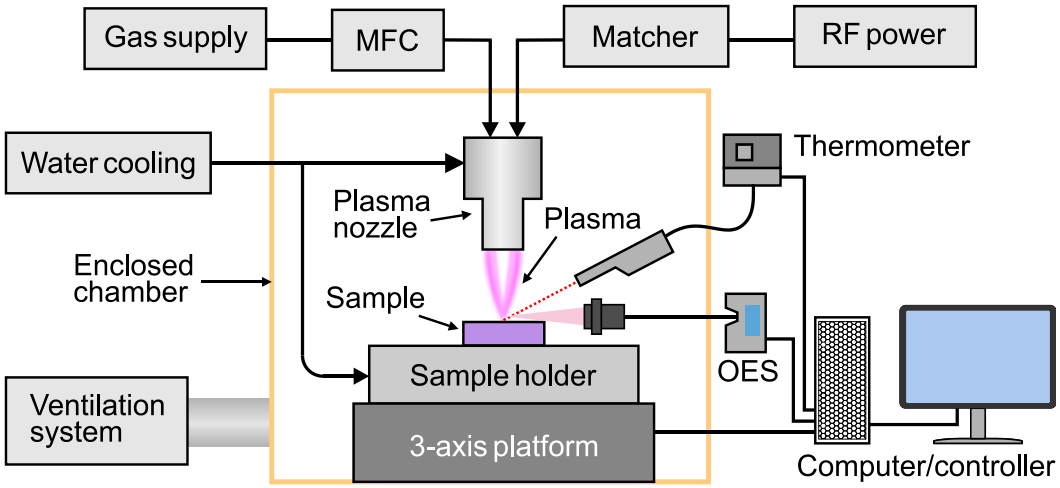


Figure 3.2 The schematic diagram of the plasma etching system

3.2.2 CCP jet nozzle

Depending on the location of the ground electrode, the CCP jet nozzle can be divided into two configurations: direct type and remote type. The ground electrode of the direct type nozzle is connected with the sample holder, whereas the remote type is located on the nozzle itself (**Figure 3.3**). For the direct type, the RF electric field is generated between the electrode on the nozzle and the sample holder, and thus plasma is also generated in the gap between them. Since the strength of the electric field is related to the electrode distance, the nozzle-sample holder spacing is critical. The empirical value is below 2 mm for the generation of stable plasma. The advantage of a direct type nozzle is that it is easy to design and fabricate, and since plasma is generated directly on the sample, it could be more reactive. However, the direct nature limits the nozzle-sample holder spacing, limiting the sample thickness below 2 mm. And the inserting of the sample will influence the dielectric

properties and the gas flow, which will influence the plasma status. Direct type nozzle is also easier to break down, leading to arc discharge that will damage the sample.

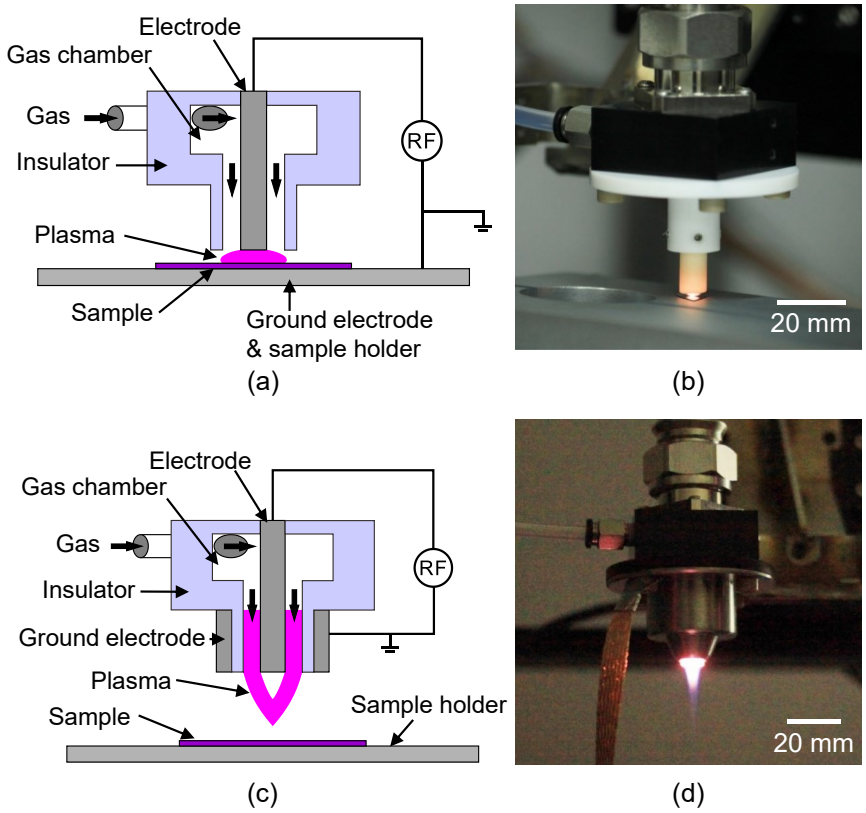


Figure 3.3 The schematic diagram and optical image of the (a), (b) direct type nozzle and (c), (d) remote type nozzle.

In the remote configuration, the ground electrode is mounted on the nozzle, and the RF electrode field is located within the nozzle. The plasma can be generated within the nozzle, and nozzle-sample holder spacing can be adjusted freely. Remote type nozzle does not require limited sample thickness; thus, it can process more complex samples. The plasma excitation region is within the nozzle; thus, it can be designed more freely and not influenced by the sample. The disadvantage of the remote type nozzle is that the concentricity of the two electrodes can be hard to manufacture, which will induce an uneven electric field and cause arc discharge. The solution uses high-precision machining and a dielectric ceramic tube between the two electrodes. Another disadvantage is that this type of nozzle can easily

accumulate heat. The thermal image of the aforementioned remote type nozzle during operation is shown in **Figure 3.4(a)**. The temperature of the centre part of the nozzle, where the plasma was generated, accumulates lots of heat. **Figure 3.4(b)** shows the maximum temperature of the nozzle during a 2 min etching process under various conditions. It can be seen that the temperature of the nozzle will increase with the power supply. And adding electronegative reactive gas will further increase the temperature. The temperature of the nozzle is very easy to exceed 300°C, and the highest temperature in the conducted operation conditions is 460.1°C. The observed high temperature is far outpacing the operating temperature of the PTFE material (polytetrafluoroethylene, -180~260°C) used as the insulator in the nozzle, which will damage the nozzle structure. Meanwhile, high temperatures will accelerate the ageing of other nozzle parts, which will change the discharge parameters and increase the uncertainty of the plasma jet. The solution is to add a water-cooling system to cool down the electrode, and the related modification has been conducted on the optimized nozzle, as described later.

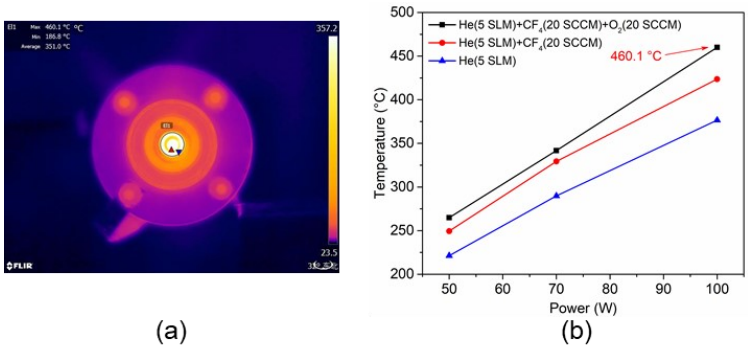


Figure 3.4 (a) The thermal image of the remote type nozzle during operation. (b) the maximum temperature of the nozzle under various operating conditions.

3.2.3 Electrode material

The material of the electrode (**Figure 3.5(a)**) can be critical for the CCP jet operation. Since CF_4 plasma is utilized, which is highly reactive, the electrode might react with the electrode and generate contamination. The electrode needs to be chemical resistant. Considering the cost and machining efficiency, two materials

have been tested: stainless steel and aluminium as the electrode material. The results are shown in **Figure 3.5(b-e)**. After etching using CF_4 plasma, the stainless-steel electrode was covered in a yellow film. In contrast, the aluminium electrode shows no visual difference after the etching.

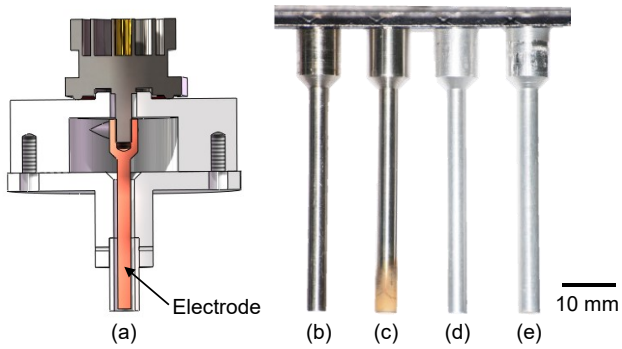


Figure 3.5 The optical image of the electrode (a) stainless-steel – before etching, (b) stainless-steel-after etching, (c) aluminium-before etching, and (d) aluminium-after etching.

The yellow film on the stainless-steel electrode after etching might consist of ferric oxide and ferric fluoride. The SEM image in **Figure 3.6** can show that the morphology changes significantly after etching, and the resulting film is fluffy. This type of film could easily drop from the electrode and lead to contamination. while in the case of the aluminium electrode, the formed alumina has been reported to be a dense film that can prevent deeper corrosion. Alumina is also a typical plasma resistance material applied in industry. Thus, aluminium is more suitable to be the electrode material in the case of CCP.

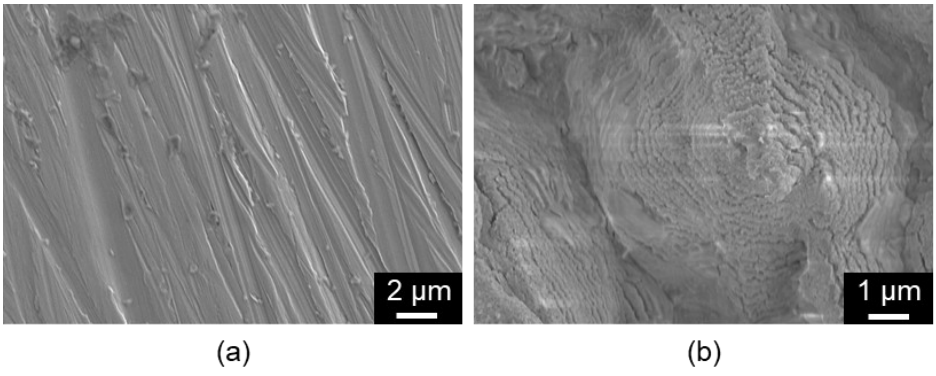


Figure 3.6 The SEM image of the stainless-steel electrode surface (a) before and (b) after etching.

3.2.4 The optimized CCP nozzle

Based on the research above, the CCP nozzle design is optimized. As shown in **Figure 3.7**, a remote type configuration has been chosen to have a more controllable plasma excitation region, resulting in a more stable plasma generation. The remote type configuration also has a huge advantage when processing complex structures as it does not limit the stand-off distance. To solve the heat accumulation problem in this configuration, a water-cooling system has been employed. The positive electrode and ground electrode have been cooled by running water separately, and the running water is then connected to a compact chiller to reduce the temperature. An alumina tube has been placed in the plasma excitation region between the two electrodes to improve the stability of glow discharge. All electrodes are made from aluminium to avoid corrosion. In addition, a replaceable spout has been mounted on the outlet of the CCP to enable us to constraint the diameter of the CCP jet.

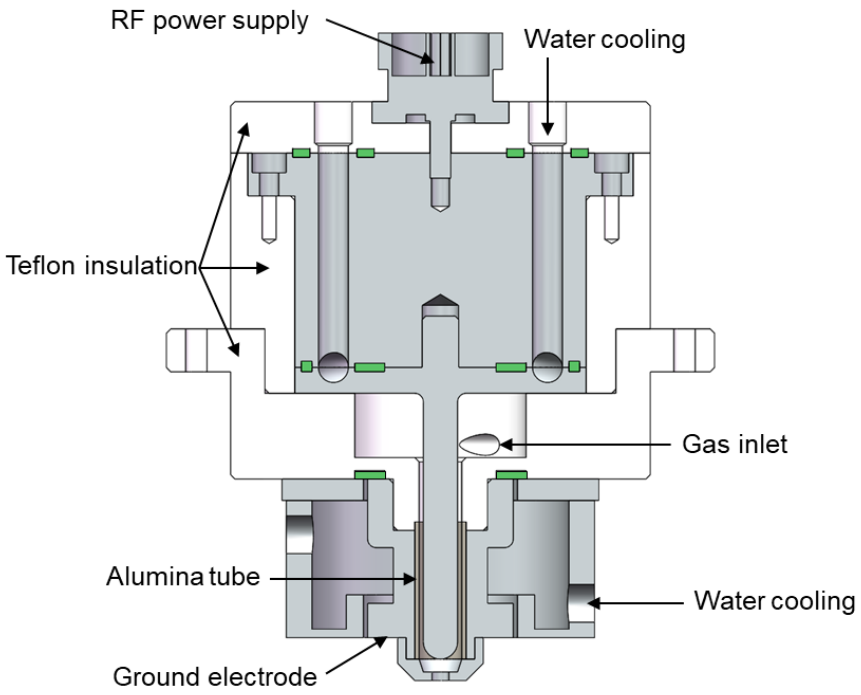


Figure 3.7 The schematic diagram of the optimized CCP nozzle.

3.3 Inductively coupled plasma (ICP) jet

3.3.1 Basic principles

The structure of the ICP jet is shown in **Figure 3.8**. ICP supplies its energy into plasma via electromagnetic induction. When an RF power supply is coupled to the RF coil through a matcher, the induced RF changing electromagnetic field will be generated in the centre of the torch. If a free electron is introduced into this region, it will be accelerated by the RF electronic field and impact other atoms and neutral molecules, forming more free electrons. The RF electromagnetic field will also generate a vortex, which will lead to lots of heat. The temperature can reach 5000-8000 K; the high heat will further accelerate the gas and transform them into plasma by thermal collision. The ICP generation device generally consists of an RF power supply, matcher, coil, and torch. The torch is usually made of quartz glass and contains three concentric tubes. The outer tube is coolant gas, preventing the high-temperature plasma from contacting the torch. The central tube is supplied with auxiliary gas, and the centre tube is reaction gas.

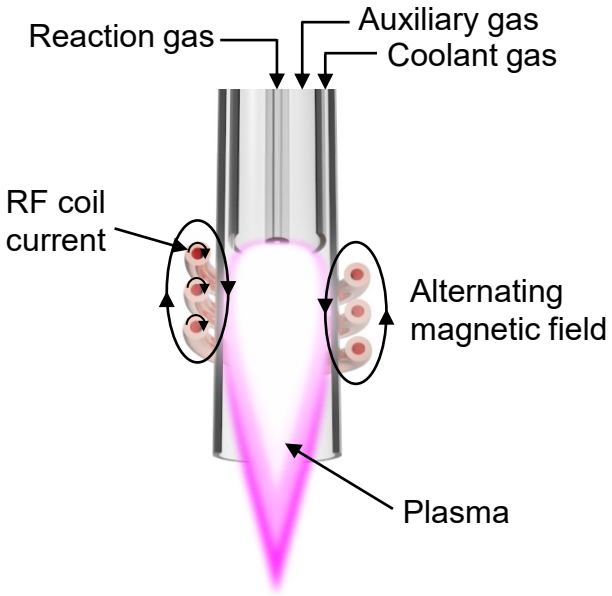


Figure 3.8 The schematic diagram of the ICP jet.

The optimum size of the coil and torch are determined by the frequency through **Equation 3.2** and **Equation 3.3** as follows.

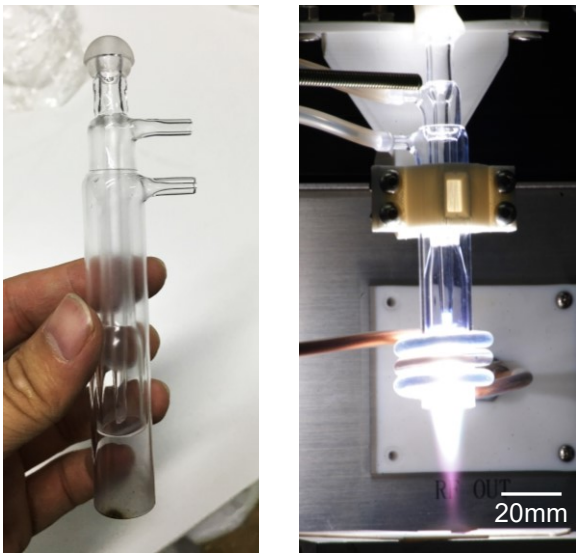
$$\delta = \left(\frac{1}{\pi\mu\sigma f}\right)^{\frac{1}{2}} \tag{3.2}$$

$$\kappa = \sqrt{2}\frac{r_n}{\delta} \tag{3.3}$$

where δ is the skin depth, μ is relative permeability, σ is the average conductivity, f is the frequency of the power supply, r_n is the radius of plasma and κ is the coupling coefficient. From **Equation 3.2**, The skin depth is constant for a determined frequency power. The optimum value of the coupling coefficient is reported to be ~1.75, and hence the optimum value of the plasma can be defined by **Equation 3.3**. The value of the external tube radius can be determined accordingly.

3.3.2 Detachable ICP torch

In the preliminary experimental study of the ICP jet, the commercially available integrated quartz torch has been used, which is widely applied in element analysis fields like ICP-OES and ICP-MS (**Figure 3.9**). This type of ICP torch is very expensive, cost about 200 GBP) each. As CF_4 gas has been used as the reaction gas, the fluorine-containing plasma is easy to etch the quartz torch and leads to damage. The operation time for each quartz torch is a few hours, the loss of the quartz torch is daunting.



(a) (b)

Figure 3.9 The optical image of the (a) integrated quartz torch and (b) the torch during operation.

In order to address the problem, a detachable ICP torch has been developed, as shown in **Figure 3.10**. The detachable ICP torch consists of three parts: quartz tube, Teflon caliper-ring, and aluminium fixture. The quartz tubes have the same diameter as the integrated quartz torch, which could ensure the coupling coefficient to be the same according to **Equation 3.3**. The commercially available quartz tube is very cheap, costing about 0.5 GBP each. Meanwhile, the length and material of the tube can be changed to meet the further requirement. For example, an alumina centre tube can resist chemical corrosion. The aluminium fixture and Teflon caliper-ring formed a self-concentric tube clamp, holding the quartz tube in the right position. With the detachable ICP torch, the torch replacement cost was reduced by one-400th of the original integrated quartz torch.

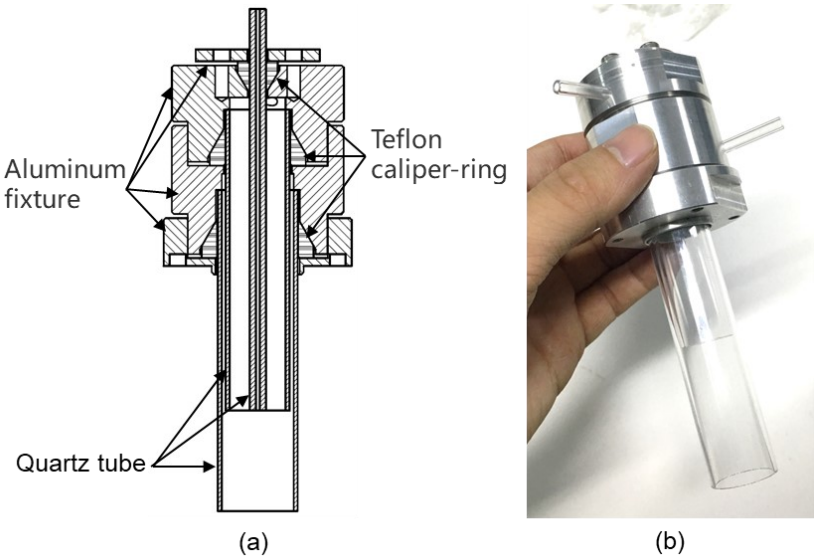


Figure 3.10 (a) The schematic diagram of the cross-section of the detachable ICP torch and (b) the optical image.

3.3.3 Sample holder

The ICP jet produces a lot of heat. The simulated temperature of the centre can reach several thousand degrees Celsius. The heat dispersion ability of the sample holder will determine the etching temperature of the sample, which greatly affects the etching performance. As shown in **Figure 3.11**, the average temperature of the sample on an aluminium sample holder is 315.7 ℃ when etched for 2 mins. When the sample holder is changed to alumina foam, which is a typical thermal isolation material, the average surface temperature reaches 1737.3 ℃. In the subsequent study, water cooling plate, graphite, quartz, and silicon carbide have been used as the sample holder to achieve multi-level temperature adjustment. As a wide range of materials has been used, some of them, such as alumina foam, are easy to introduce dust contamination on the sample surface. Hence a piece of 2 mm quartz glass has been placed between the sample and sample holder that significantly reduced the contamination.

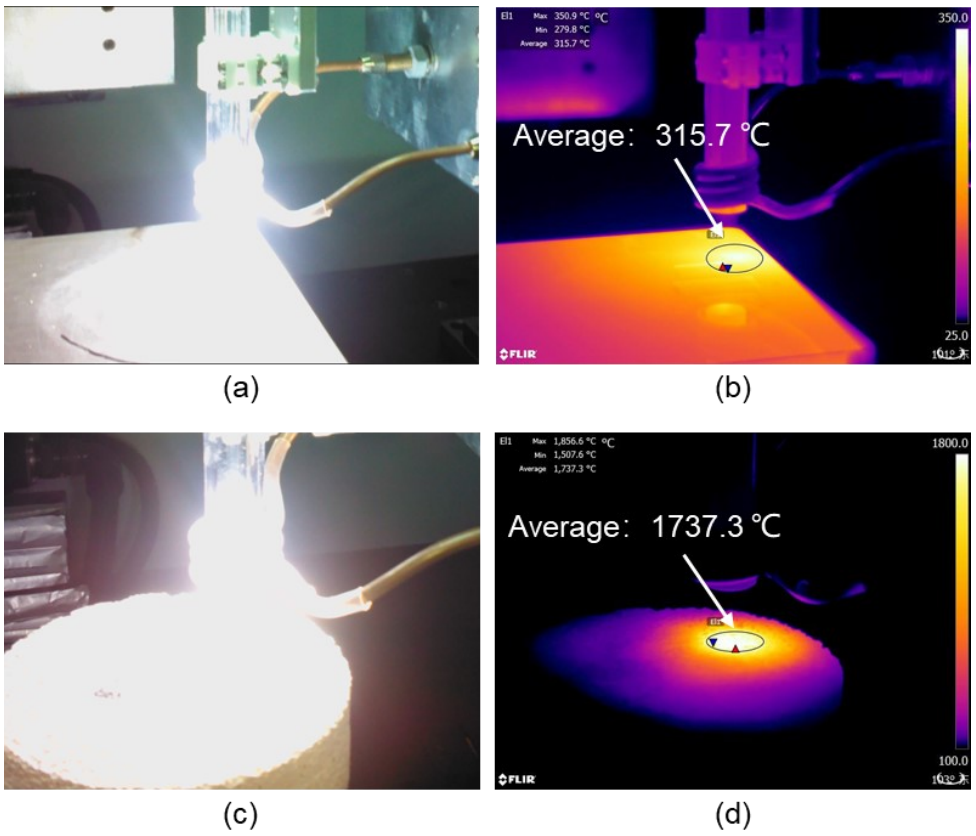


Figure 3.11 The optical and thermal image of ICP etching on (a), (b) aluminium sample holder, and (c), (d) alumina sample holder.

3.3.4 Environmental control strategies

During ICP jet etching, atmospheric gases, such as O_2 and N_2, are likely involved in the reaction. The unwanted oxide and nitride are often observed. The sample after etching can be very hot, it is likely to react with the ambient O_2 due to thermal oxidation after the plasma is turned down. To solve the problem, several environmental control strategies have been tried.

The first solution, as shown in **Figure 3.12**, is moving the torch closer to the sample immediately after turning down the plasma. The argon gas flow keeps running for several minutes to cool the sample and avoid ambient gas contacting the sample. This method is simple and effective in avoiding thermal oxidation after the plasma is turned down. However, this method cannot prevent the contact of ambient gas during the etching operation. The second solution uses a shield system

made with quartz glass and aluminium, as shown in **Figure 3.13**. A water-cooling system is added as the quartz shield will accumulate lots of heat. A gas exhaust pump was connected to the shield, prevent ambient gas from reaching the centre etching zone. This system is supposed to protect the etching process. However, unpredictable arc discharge is often observed during the operation, making the etching process unstable.

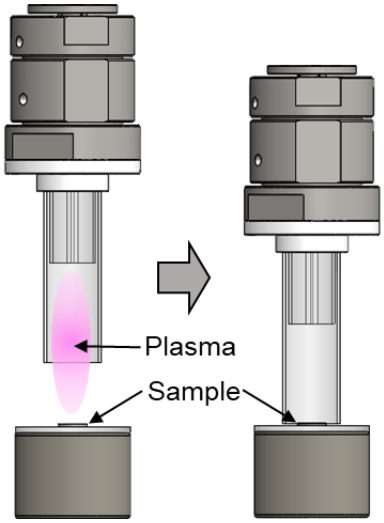


Figure 3.12 The schematic diagram of the first environmental control solution.

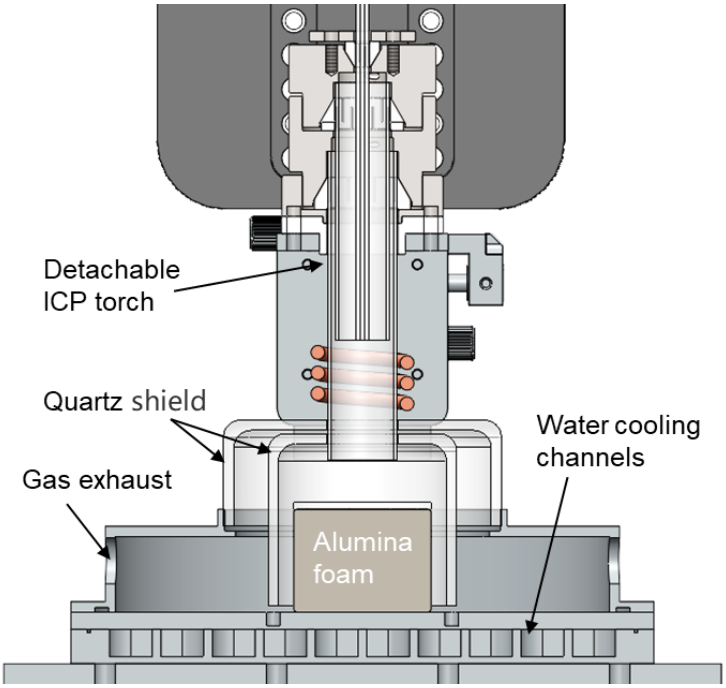


Figure 3.13 The schematic diagram of the second environmental control solution.

The third environmental control solution is more traditional, using a vacuum chamber. The schematic diagram of the experimental setup is shown in **Figure 3.14**. The ICP torch system and 3-axis numerical control platform have been put into a vacuum chamber. The operation process is: 1. Put the sample on the sample holder and close the vacuum chamber. 2. Generate vacuum in the chamber. 3. Blow-in nitrogen to increase the pressure inside the vacuum chamber to atmospheric pressure. 4. Open the ICP torch and perform the etching process after achieving the atmospheric pressure. 5. After etching, close the ICP torch, again generate vacuum in the vacuum chamber and wait for the sample to cool down to room temperature. 6. After the sample cools down, inject air to return to atmospheric pressure, open the chamber and collect the sample. This method can prevent oxidation after etching. However, this setup cannot solve the nitrogen contamination problem as nitrogen is needed to pressurize the chamber. And if the argon has been used as the pressurized gas, the plasma could not ignite properly.

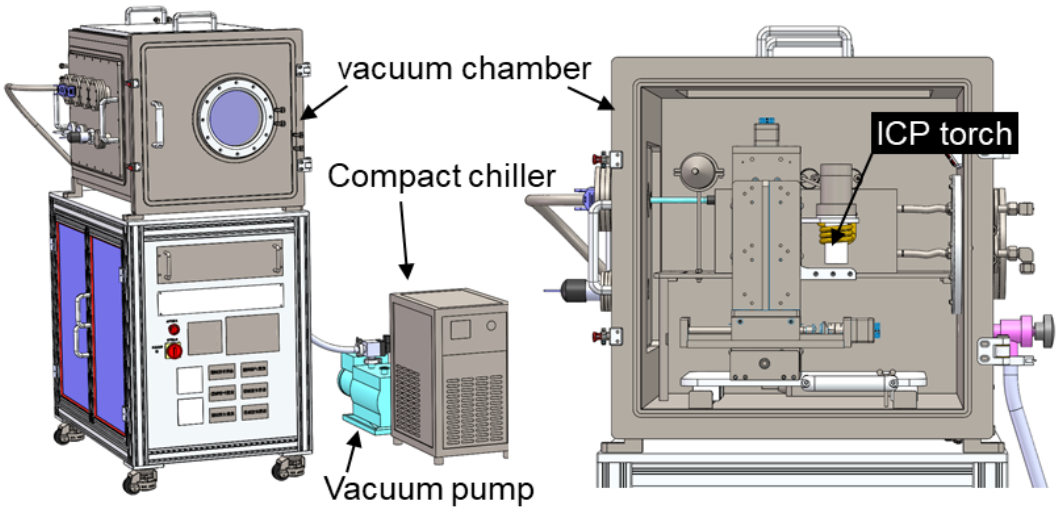


Figure 3.14 The schematic diagram of the ICP system with a sealed cavity.

3.4 Ultrahigh temperature molten KOH etching [134]

Molten KOH can quickly react with many chemical-resistant materials, including many third-generation semiconductor materials studied in this thesis. As a pure

chemical reaction, molten KOH etching can help to study the atom selection etching effect. Thus, a KOH etching system has been built to work under a wide temperature range. As shown in **Figure 3.15,** conventional molten KOH etching put the sample and KOH powder in a nickel crucible and heated them using a muffle furnace. However, this setup is not suitable for ultra-high temperature operation. Nickel crucible will react with high-temperature molten KOH. Meanwhile, it takes a long heating time for the muffle furnace to reach a high temperature, which leads to over-etching of the sample.

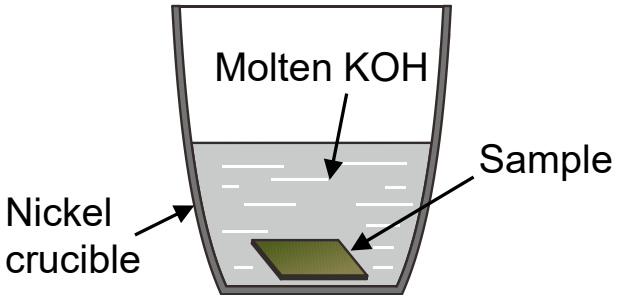


Figure 3.15 The schematic diagram of the conventional molten KOH etching process. [134]

Heating and etching the sample using ultrahigh temperature molten KOH with conventional nickel crucible can be operated in three ways. The first option is to directly put the sample and KOH into the nickel crucible and then place them into a muffle furnace and go through the whole heating process. This process is easy to operate. However, hours of heating will lead to serious over-etching. Meanwhile, when operated at a high temperature (> 900 ℃) for a long time will evaporate most part of the KOH. The second option contains two steps. First, preheat the nickel and KOH to the target temperature, then use a platinum sample holder to hold the sample and put the sample into the molten KOH for etching; after etching, remove the sample out of the KOH using the platinum sample holder. The method works well under 900 ℃. However, the large amount of KOH vapour generated above 900 ℃ makes the sample loading and unloading process very dangerous. The third option contains two steps, first, preheat the maffle furnace to the target high temperature; then, place the crucible, which contains the sample and KOH powder,

into the furnace for etching. Nevertheless, heating the crucible and the KOH is not fast enough. Over a high-temperature range (> 900°C), reactions occur between nickel and molten KOH, and the sample becomes highly polluted with reaction products. To overcome those problems, a crucible-less molten KOH etching method has been developed.

The schematic diagram of this method is shown in **Figure 3.16**. Similar to the aforementioned third option, the muffle furnace is preheated to the target temperature. A small sheet of solid KOH (~0.05 g) was directly placed on the Si face of the sample. After that, the sample stack was placed on the top of an adiabatic stage for easier grip. The sample stack with the adiabatic stage is transferred to the furnace when the target furnace temperature is achieved. Solid KOH is quickly heated to the target temperature due to the small mass, forming a molten KOH droplet covering the whole Si face of the SS-SiC chip, and etching reactions occur. This method provides the fastest approach to heat KOH to the target temperature without crucible pollution. After the etching reached the target time, the sample stack was removed from the furnace and directly cooled in the atmosphere. The practical etching temperature using this method can reach 1200 °C, which meets the requirements properly.

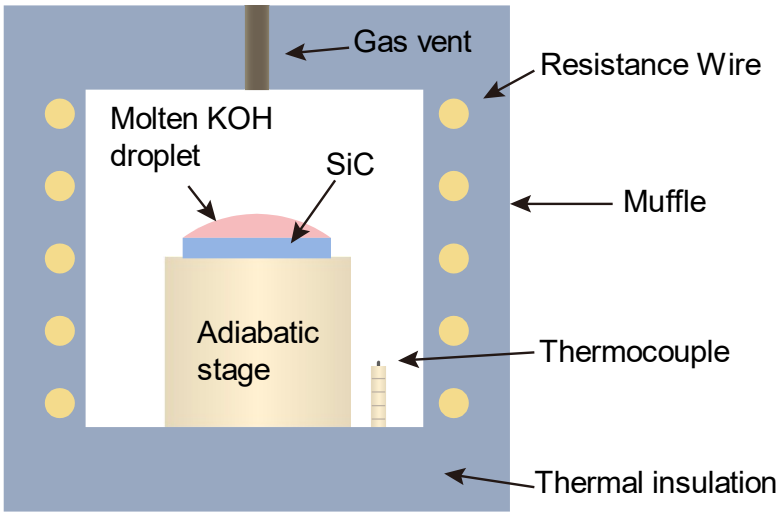


Figure 3.16 The schematic diagram of the crucible-less molten KOH etching setup. [134]

3.5 Summary

In this chapter, the background of three groups of etching apparatus, including CCP etching, ICP etching, and KOH etching, have been introduced, and their optimization processes have been investigated for practical applications.

(1) The CCP etching device has been developed for low-temperature etching. The configuration, electrode material, and cooling system have been studied for the optimal device, which has utilized the remote type nozzle with aluminon electrode material and a water-cooling system.

(2) The ICP etching device has been developed for high-temperature etching. A detachable ICP torch has been built to reduce the cost. Then, different sample holders have been made to control the sample temperature. Also, several environmental control strategies have been developed to prevent contamination from the ambient atmosphere.

(3) The crucible-less ultra-high temperature KOH etching device has been developed to further test the etching properties under a wide range of temperatures. The experimental setup has offered a fast approach to etching at 1200 °C without pollution from the crucible.

Chapter 4

Plasma-based atom selective etching (PASE) demonstration

4.1 Introduction

This chapter provides a successful demonstration of PASE on SiC. After testing various plasma sources, ICP exhibits the ability to realize PASE. The demonstration was based on the ICP jet introduced in **Section 3.3**, and the schematic of the setup is shown in **Figure 4.1**. Plasma diagnostics is conducted to confirm the radical species that ensure the reaction has been performed. The typical PASE morphology is discussed and observed, confirming the atom selective etching. The polishing ability of PASE is evaluated by roughness and MRR, and a comparison is conducted between PASE and other ultra-precision polishing methods introduced in **Chapter 2**. Furthermore, PASE is performed on various substrates to demonstrate its universality.

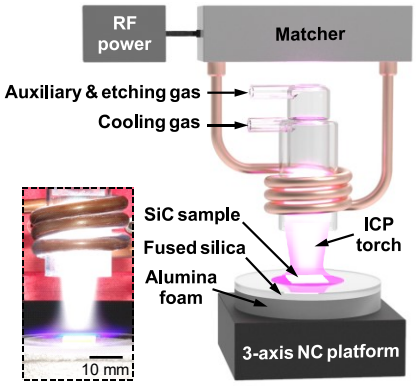


Figure 4.1 The schematic of the PASE setup

4.2 Plasma diagnostics [135]

The plasma etching of SiC is based on the chemical reaction expressed as **Equation 4.1** [136]:

$$SiC + mF + nO \rightarrow SiF_m + CO_n + CF_m \ (m = 1 \text{ to } 4, n = 1 \text{ to } 2) \qquad (4.1)$$

According to this equation, fluorine and oxygen radicals are involved in the etching of SiC. The reactive plasma must contain sufficient amounts of F and O radicals to ensure that the reaction can proceed. Thus, plasma diagnostics of plasma sources were implemented before the etching operation.

An optical photo of the ICP jet is shown in **Figure 4.2(a)**. OES has been used to confirm the presence of etching radicals in the plasma. OES data were collected from the normal analysis zone (NAZ) of the ICP jet, and the results are shown in **Figure 4.2(b)**. When CF_4 was added to the plasma, distinctive peaks corresponding to CF_X and the typical C_2 swan system were observed [137-139]. The peaks representing fluorine radicals are difficult to detect because they overlap with the strong peaks of argon emissions. However, the strong peaks of CF_X and C_2 prove the sufficient dissociation of CF_4, which generates a substantial amount of fluorine radicals as another major product [140]. The atomic oxygen peaks at 777 nm and 844 nm represent the transitions O (3p5P→3s5S) and O (3p3P→3s3S), respectively [141]. The OES results indicate that this ICP jet contains F and O radicals in abundance which are capable of etching SiC.

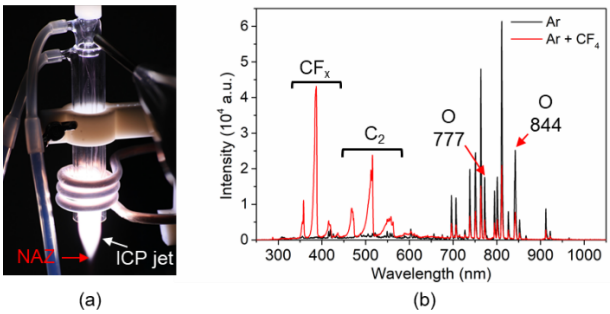


Figure 4.2 (a) Optical photo of the ICP jet; (b) OES spectra of the ICP jet with and without CF_4 addition. [135]

A thermal camera (FLIR T660) has been used to evaluate the temperature of the SiC samples during plasma etching. The emissivity of the SiC sample has been calibrated using the contact thermometer method: placing a SiC sample on a heated table and increasing the temperature to a higher value. When the temperature is stable, a thermocouple and a thermal camera measure the temperature of the same spot at the same time. Based on the different temperature measurements, the emissivity correction could be achieved. After that, the thermal camera is calibrated and can be used to measure the temperature of SiC samples accurately.

As described in **Section 3.3.3**, high etching temperature of over several hundred degrees to thousand degrees can be obtained by ICP with various sample holders. For the case of the PASE demonstration, an alumina sample holder is employed. The heating curve of the sample on the alumina sample holder is shown in **Figure 4.3**. The sample temperature will quickly rise to over 1400°C in 60 seconds; the heating rate is much higher than conventional furnaces or heating tables. The temperature can be regulated by modulating the power and stand-off distance. After it has been etched for the set time, the ICP will be turned off, and the sample will be rapidly cooled under the shielding of Ar flow.

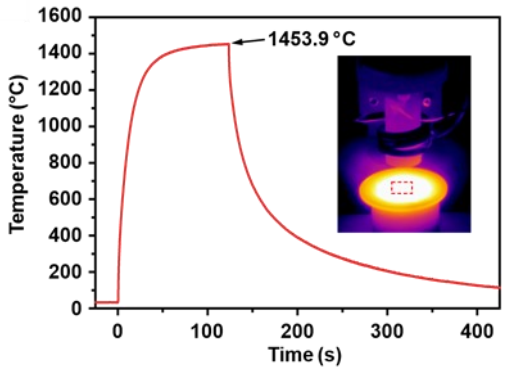


Figure 4.3 The hearting curve of PASE demonstration.

4.3 Etching characteristics

Based on the mechanism proposed in **Chapter 2**, a simple simulation was done to predict the morphological changes. As shown in **Figure 4.4**, a 2D pixel map has

been used to represent the cross-sectional profile of a rough crystal material. The violent fluctuations on the upper part of the pixel map represent the surface damage. The zoom-in picture is shown on the right. The black pixel layer represents the atom layer of a single crystal material. When etching was conducted on the surface, the etching effect can be separated into two directions. The etching along the vertical direction is v_0, while the lateral direction is v_L.

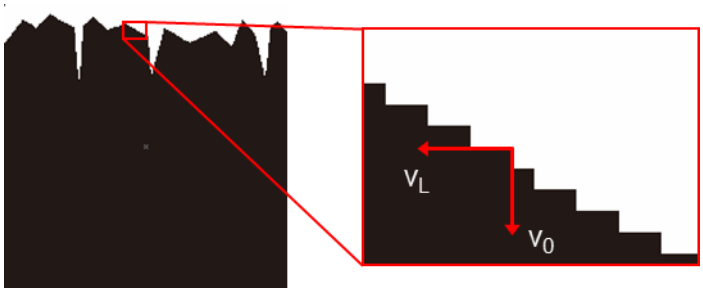


Figure 4.4. The schematic diagram of the simulation module.

When the PASE effect occurs, selective etching of the edge of atom step happens, the relationship between etching alone lateral and vertical direction can be approximated as $v_L >> v_0$. The morphology change of the surface has been simulated, as shown in **Figure 4.5**. When $v_L >> v_0$, a typical lateral etching mode dominates, the crack on the surface will be etched along the lateral direction rather than the vertical direction. Thus, the crack will not be deeper but become wider and wider. As the bottom of the crack stop propagating in the vertical direction but is etched along the lateral direction, a typical flat-bottom morphology emerges. The protrusions on the surface, which constitute the surface roughness shrink rapidly and disappear with lateral etching. The flat-bottom morphology should be the iconic phenomenon during PASE.

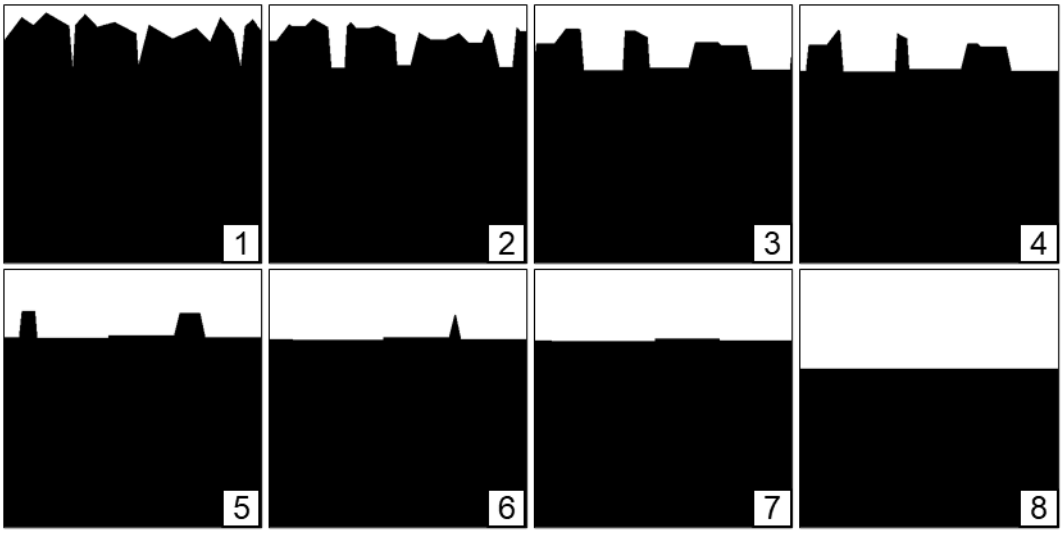


Figure 4.5. The simulation of the morphology changes under PASE.

The demonstration of PASE has been conducted on commercially available sliced 4H-SiC on-axis substrate (S-SiC) with experimental conditions listed in **Table 3**. The results from the PASE demonstration experiment are shown in **Figure 4.6**. The surface of the as-received sliced sample shows a typical damaged morphology. Brittle fracture introduced by slicing can be observed. When PASE starts, the surface crack rapidly expands in the lateral direction while remaining relatively slowly in the vertical direction. After 3 seconds, the cracks become even more border and shallower due to the merging of lateral etching. The high-frequency roughness on the as-received surface has also been removed. The typical flat-bottom morphology emerges and becomes very obvious in the 10 s etched sample, conforming to the lateral etching effect. The flat bottom continually expands and finally combines with the ongoing etching. Meanwhile, the surface protrusions shrink rapidly and disappear, forming an integral flat surface without any step and terrace, as observed in the 1 min etched sample. This set of samples could clearly state that PASE can achieve the lateral etching effect and polish the sample efficiently. To further prove the finding, the sample profile has been measured with AFM, as shown in **Figure 4.7**. **Figure 4.7(a)** is the profile of the as-received sliced surface; a very rough structure introduced from machining can be observed. The profile of the 3 s and 10 s etched sample is shown in **Figure 4.7(b)**

and **Figure 4.7(c)**, respectively, the high-frequency rough structure of the machining has been removed, and an opening of crack can be found. The typical flat-bottom morphology can also be observed in **Figure 4.7(c)**, confirming that the PASE effect has been obtained successfully. With the extension of etching duration, the surface has been eventually flattened, as shown in **Figure 4.7(d)** of the profile of the 5 min sample. The result listed below implies that PASE has been achieved, and it is a potential ultra-precision polishing method with ultrafast speed.

Table 3 Conditions of PASE demonstration

Parameters	Value
Specimen	10×10 mm n-type sliced 4H-SiC, on-axis
Reaction gas	CF4 (30 SCCM), O2 (20 SCCM)
Coolant gas	Argon (18 SLM)
Auxiliary gas	Argon (1.5 SLM)
Duration time	1s ~ 20 min
Stand-off distance	18 mm
Sample holder	Alumina 50 mm

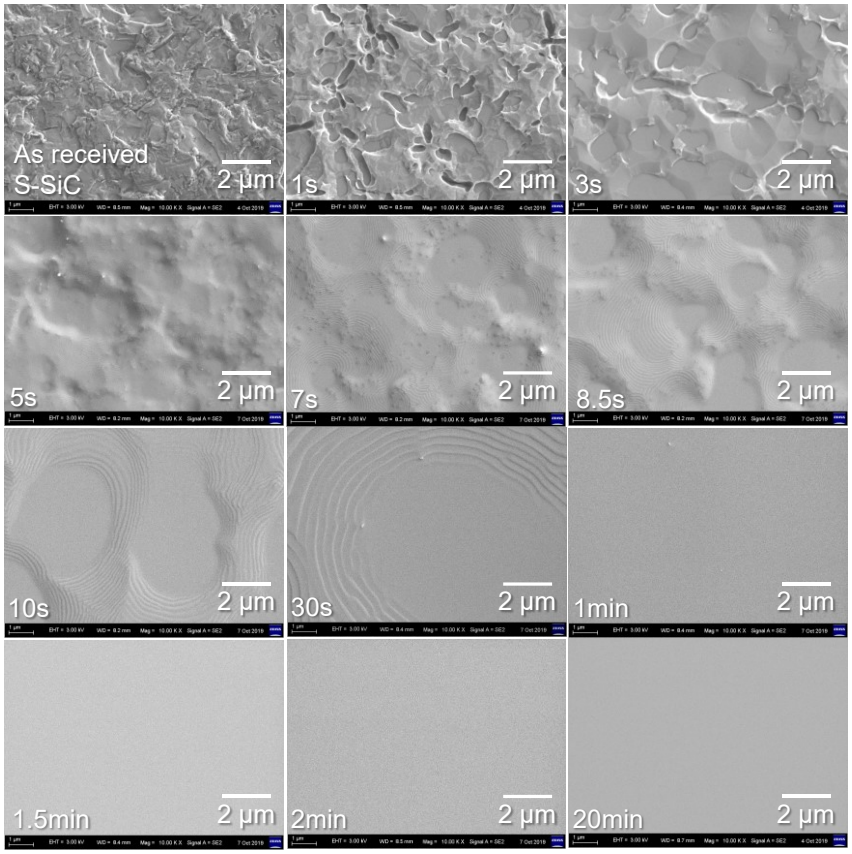


Figure 4.6 The SEM image of the SiC sample etched by PASE

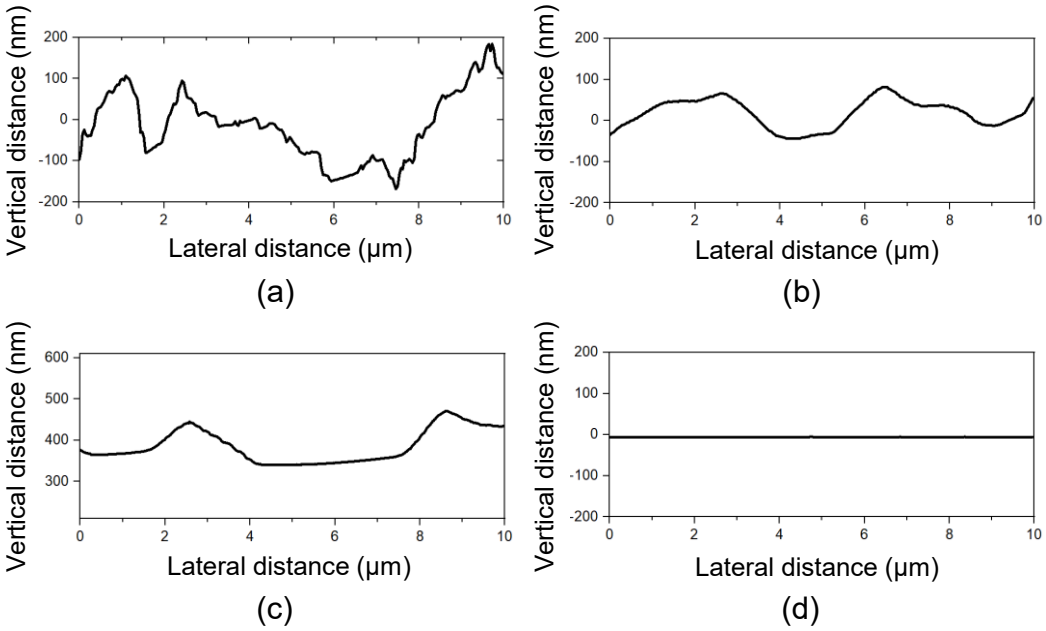


Figure 4.7 The profile of the SiC sample etched by PASE. The etching durations are: (a) 0 s (as-received), (b) 3 s (c) 10 s and (d) 5 min.

4.4 Truly-atomically flat surface

PASE has been found to have a strong polishing effect as inferred from the previous section; hence the roughness change during PASE is valuable to be studied in detail. The experimental condition is the same with **Table 3**. AFM has been employed to study the roughness, and the results are shown in **Figure 4.8**. The AFM image verified the flat-bottom morphology; the 10 s etched sample shows the most typical morphology. The roughness reduced from 92.3 nm to below 1 nm in 60 s and convergence to sub 0.1 nm in 5 min. After that, the roughness remains unchanged in the sub 0.1 nm range with the extended duration.

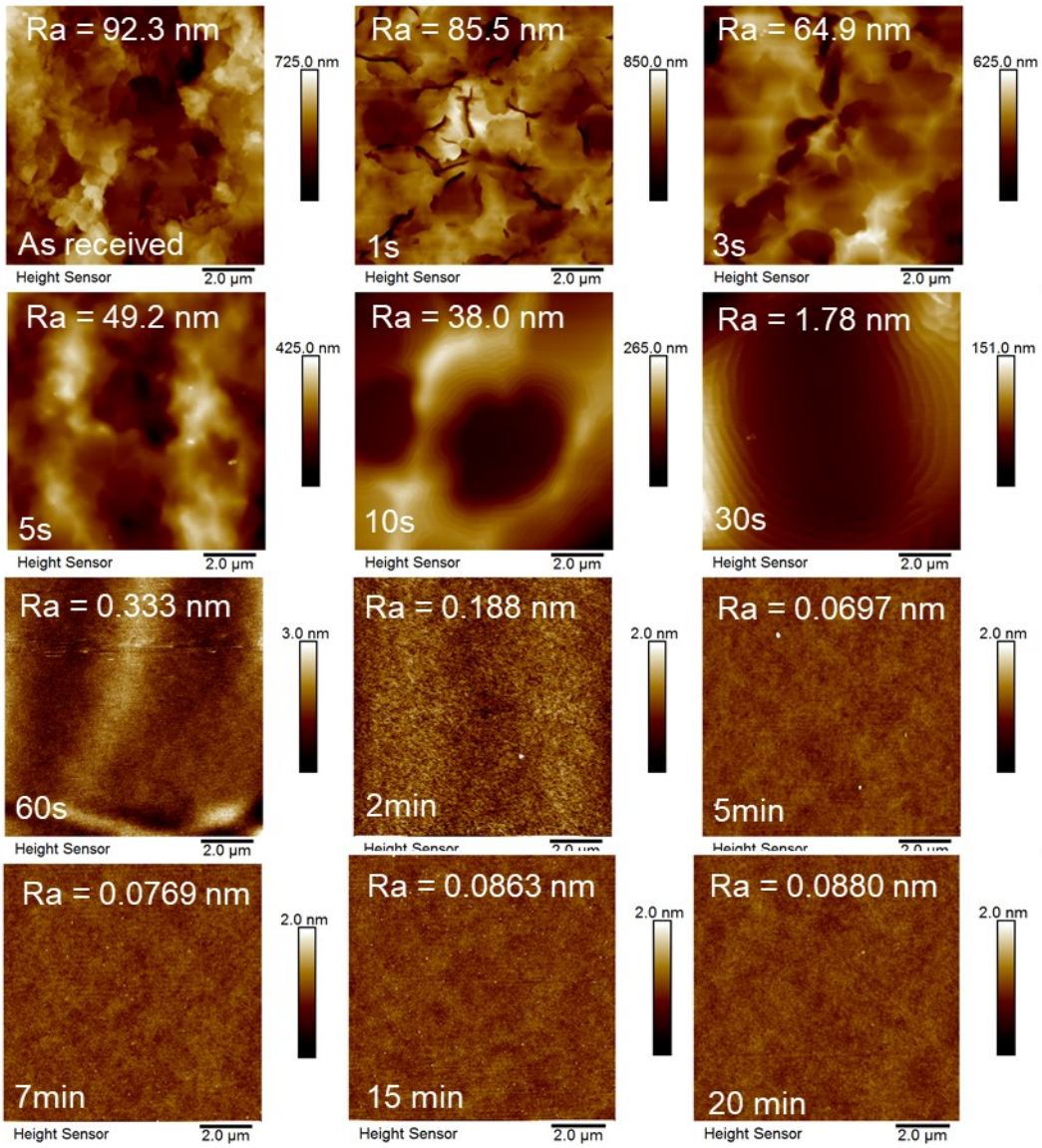


Figure 4.8 The AFM images of the SiC samples etched by PASE

The power spectral density (PSD) curve has also been employed to study the roughness change. **Figure 4.9(a)** shows the PSD of the SiC sample etched by PASE with increasing duration. The PSD reduced rapidly with even seconds of processing and eventually converged after just 5 min. This result suggests PASE can reach the polishing limit in just 5 mins, which often takes hours for the conventional CMP method. The comparison of PSD between the as-received sliced sample to the sample PASE for 5 mins shows an improvement of all spatial frequency, implying PASE has a broad-spectrum polishing effect. The final roughness is converged to the atomic level, which is also the limit of polishing technology.

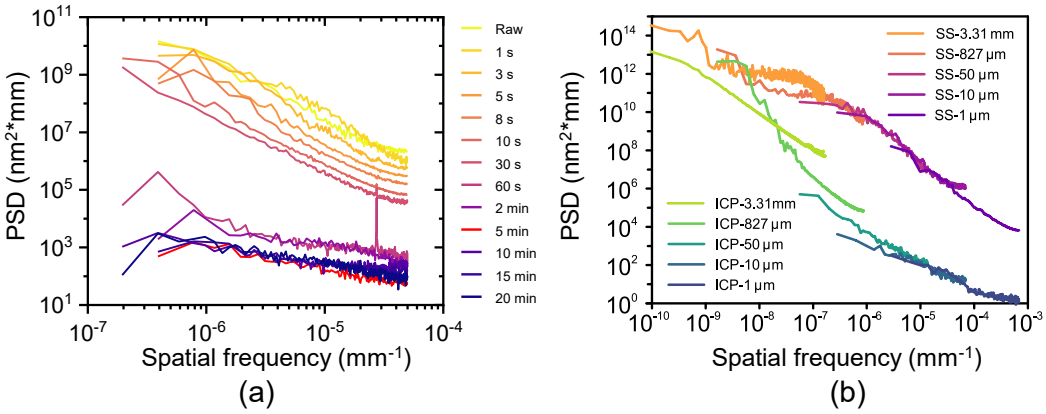


Figure 4.9 The PSD curve of (a) SiC sample polished by PASE with different duration, (b) the comparison between as-received sample to the sample PASE for 5 min.

Although the roughness of the etched sample can reach atom level roughness, the atom steps, which are often seen in other high precision polishing methods, have not been observed, as shown in **Figure 4.10**. There could be two possible explanations. First, the whole surface is within one single atom step terrace. This means the surface has achieved a truly-atomically flatness; thus, atom steps could not be observed. The second reason is that an amorphous layer might cover the surface, and the amorphous surface does not have an atom step. To avoid the second possibility, high resolution transmission electron microscopy (HRTEM) of the cross-section of the etched sample has been performed to observe the state of the surface layer.

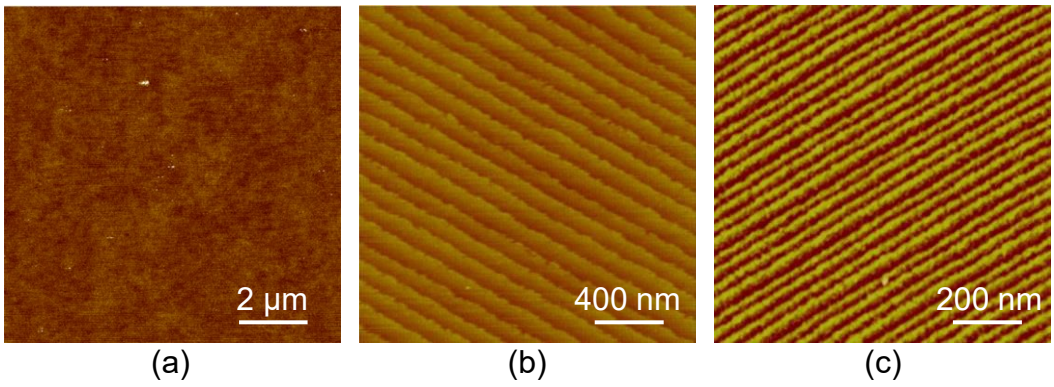


Figure 4.10 step and terrace structure on SiC surface polished by (a) PASE, (b) CMP, and (c) PAP [142, 143].

The TEM sample was prepared using a focused ion beam (FIB). Since the FIB is easy to induce damage and produce an amorphous layer on the sample surface, The surface of the sample has been carefully protected before FIB: A layer of electron beam evaporated Cr (EBE-Cr) with a thickness of 80 nm has been deposited on the SiC surface to protect the sample. The EBE-Cr is believed to have no damage to the substrate, and the good crystallinity can distinguish the protection layer from the potentially existing surface amorphous layer. The other two Pt protection layers deposited using ion-beam included deposition (IBID) and electron-beam induced deposition (EBID) has been used to provide further protection, as shown in **Figure 4.11(a)**. The HRTEM image of the interface is shown in **Figure 4.11(b)**. A very clear Lattice structure of SiC and EBE-Cr can be observed. No amorphous layer can be seen between them, suggesting no amorphous deposition or damage layer remains on the PASE etched surface. Hence the roughness obtained by AFM is the real roughness of the SiC substrate.

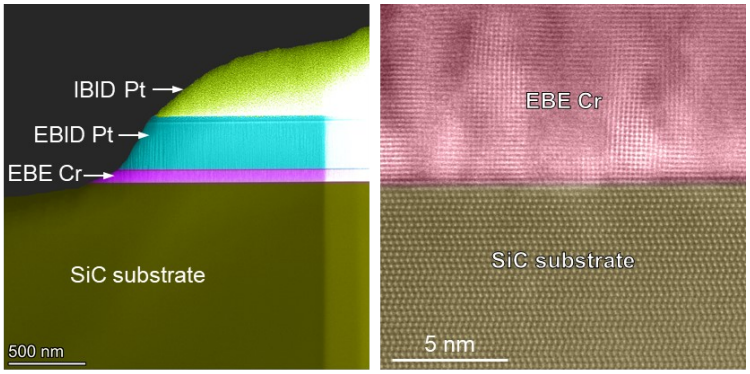


Figure 4.11 (a) the TEM image of the cross-section of the PASE polished SiC, (b) The HRTEM image of the interface area of the sample.

The situation of the top-most layer of the SiC atom still cannot be confirmed in the sample before. Because the low electron transmittance of Cr makes the brightness of the Cr protection layer higher than the SiC substrate, it makes it harder to identify the SiC. Meanwhile, the interference between the lattice of Cr and SiC also makes it harder to observe the top-most layer of SiC. To identify the first layer of SiC clearer, the EBE-Cr has been replaced by a painted carbon layer. The result is shown in **Figure 4.12**. The top-most atom layer of PASE polished SiC is a continuous atomic layer without any observed atom missing or atom step. This result suggests that the PASE polished surface with atomic level roughness observed by AFM aforementioned could be truly-atomically flat without any atom steps. PASE is demonstrated to be a novel polishing method that can achieve ultra-low roughness, likely truly-atomically flat surface, with ultra-high speed.

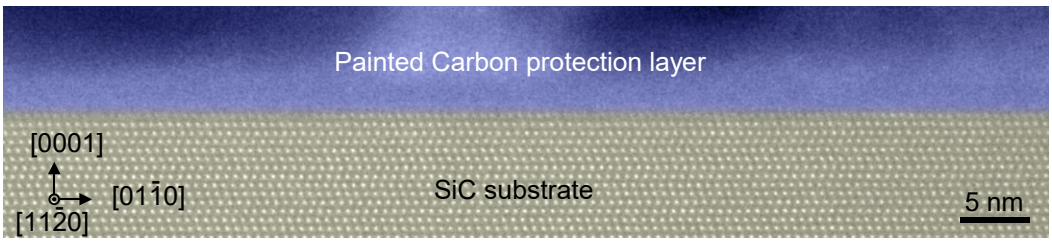


Figure 4.12 The HRTEM image of the cross-section of the surface of the PASE polishing SiC.

4.5 Material removal rate (MRR)

Since the polishing speed observed in the previous section has been so high,

polishing the SiC sample from 92.3 nm to sub-1 nm in 1 min, the MRR of PASE should be remarkable. The MRR (μm/min) is calculated by weight difference of the sample before and after PASE using a precision weighing machine (least count = 0.1 mg). The Equation used for calculating MRR is as under:

$$\mathrm{MRR} = \frac{\Delta h}{t} = \frac{\Delta m}{S\rho t} \tag{4.2}$$

where Δh is the thickness difference of the sample before and after PASE, t is the duration time, Δm is the weight difference, S is the basal area of the sample, ρ is the density of the sample. Since the basal area can be hard to measure precisely, the combination of **Equation 4.2** and **Equation 4.3** provide **Equation 4.4**:

$$m = hs\rho \tag{4.3}$$

$$\mathrm{MRR} = \frac{\Delta m h_0}{m_0 t} \tag{4.4}$$

where h_0 and m_0 are the thickness and weight of the as-received sample, respectively, the height and weight are easier to measure accurately than the basal area. The MRR calculated using this measure is shown in **Figure 4.13**, together with roughness changes. During the first minute of etching, the roughness rapidly decreases from 92.3 nm to sub-1 nm, and then slowly reduces to ~0.05 nm in 5 mins and converges at that roughness. The MRR decreased from ~90 μm/min to ~35 μm/min in the first minute and then converged to ~ 30 μm/min. PASE polishing is based on the selectively etching of SE-atoms, which can also be interpreted as a much higher lateral etching speed than vertical. This means the MRR should be closely related to the surface roughness as higher roughness implies more exposed atom step-edges. These results also prove the atom selective etching mechanism of PASE.

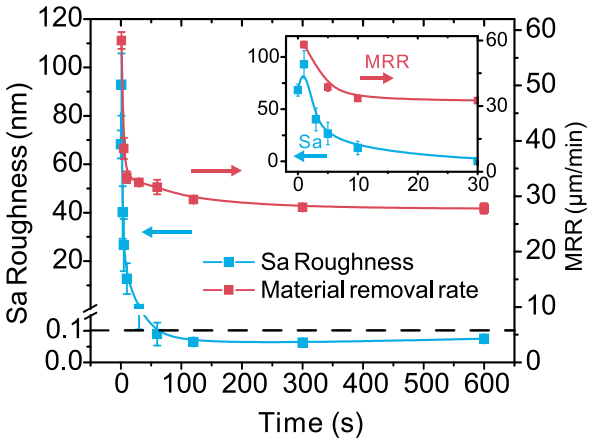


Figure 4.13 The roughness and MRR change with PASE duration time.

The MRR and roughness under various conditions have also been tested, as shown in **Figure 4.14**. It can be seen that the MRR increases with power and CF_4 flow. Meanwhile, the roughness is almost the same for different MRR. This is very different from other mechanical-related methods, where higher MRR often results in a rougher surface.

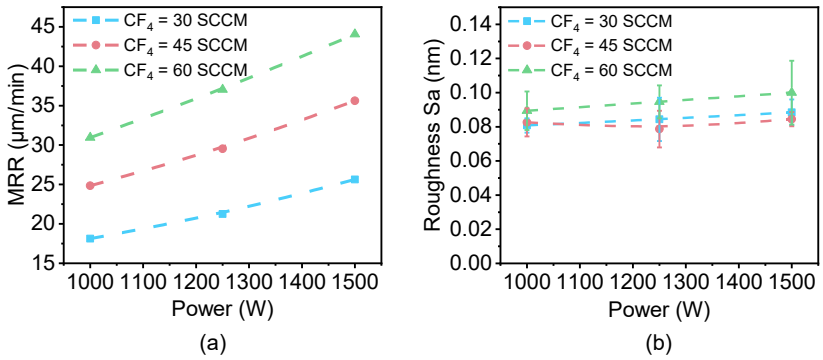


Figure 4.14 (a)The MRR and (b) roughness under different PASE conditions.

The outpacing MRR suggests PASE could be a unique method compared to other ultra-precision polishing methods. Here, PASE is compared to the mainstream and cutting-edge methods applied in polishing SiC listed in **Table 2** (**Figure 4.15**). PASE method can achieve the lowest roughness, while the speed exhibited three orders of magnitude higher than the close method. Meanwhile, PASE is theoretically possible to achieve truly-atomically flatness of which, other methods are not capable. PASE also overruled the conception that high MRR will result in a rough surface; when MRR increases in PASE, the roughness remains almost the same.

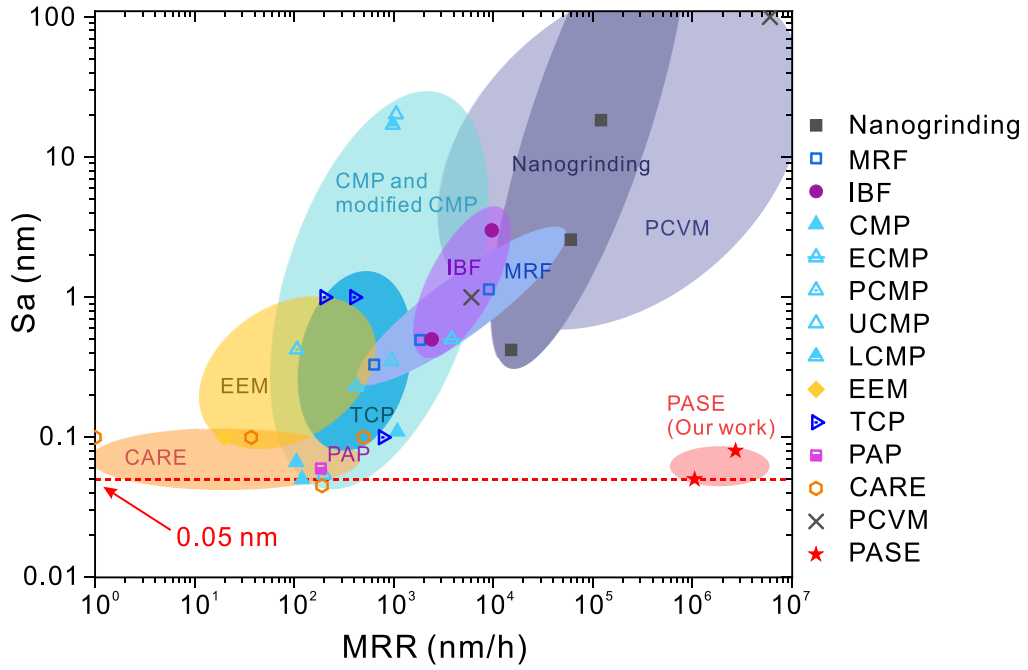


Figure 4.15 The comparison between PASE and other ultra-precision polishing methods.

4.6 Universality of PASE

The generic ability of the PASE method has been further demonstrated. Theoretically, it could polish any single crystal material with atomic steps. Since difficult-to-machine materials urgently need a high MRR polishing method, the typical difficult-to-machine materials have been listed in **Table 4** to facilitate the screening of test materials. PASE can machine a material that have a high melting point since PASE is operated at a high temperature (>1200 °C). Meanwhile, the material should react with the reagent gases in the plasma, here CF_4 and O_2 are the only considered reagent gas due to their availability and low toxicity. Also, the reaction product should have a boiling point lower than the PASE operating temperature to exclude the reaction produce efficiently. Last but most important, the material should be a commercially available single-crystal wafer. Based on **Table 4**, several typical difficult-to-machine materials (Si, Al2O3, AlN, GaN) were chosen to be the material to test the universality of the PASE method.

Table 4 Properties and availability of difficult-to-machine single-crystal materials.

Sample	Si	SiC	Si_3N_4	Al_2O_3	AlN	GaN	C-BN	B_4C	WC	ZrO_2	ZrC	TiN	TiC	TiB_2	ReB_2	CBe_2	TaC	Diamond
Mohs hardness	7	9.2	8.5	9	9	9	10	9.3	9	8.5	9	9	9	9.5	9.5	9	9	10
Coefficient of thermal expansion (10^{-6}/K)	2.62	2.5-4	1.4-3.7	7.5	4.84	5.59	2	4.2-4.6	4.5-7.1	2.3	6.6-6.8	/	7.4	6	/	/	/	1.2-4.5
Melting point (°C)	1410	2700	1900	2040	2750	1700	3000	2763	2785	2715	3532	2947	3160	3230	2400	2100	3850	3550
Reagent gas	CF_4	CF_4	CF_4	Cl_2, BCl_3, CF_4	Cl_2, BCl_3, CF_4	Cl_2, CF_4	CH_4, H_2, Cl_2	CF_4	CF_4	CF_4	CF_4	CF_4	CF_4	CF_4	CF_4	CF_4	CF_4	O_2
Product	SiF_4	SiF_4	SiF_4	AlF_3	AlF_3	GaF_3	BF_3	BF_3	WF_6	ZrF_4	ZrF_4	TiF_3	TiF_3	TiF_3, BF_3	ReF_6	BeF_2	TaF_5	CO, CO_2
Boiling point of product (°C)	-86	-86	-86	1291	1291	1000	-100.3	-100.3	17.1	905	905	1400	1400	1400	221.3	1175	229.5	-78.5
Availability of single-crystal wafer	✓	✓	×	✓	✓	✓	×	×	×	✓	×	×	×	×	×	×	×	✓

Figure 4.16 shows the morphological changes of the selected material undergoing PASE. All the materials reached atomic flatness from the sliced raw surface in minutes. Many of them have observed the typical flat-bottom morphology during the etching process. The TEM image of the PASE polished Si and Al_2O_3 are shown in **Figure 4.17**. The clear lattice structure can be observed, suggesting the PASE has achieved a real polishing effect, and the low roughness measured by AFM is the real roughness of the polished substrate. It is notable that the optimized conditions for different materials vary because of the reaction paths and activities. The optimized conditions for the tested material are listed in **Table 5**. Here, the empirical method was employed to find the optimized condition with low efficiency. It will be valuable to find a universal prediction method to optimize the working conditions for the PASE of new materials, which suggests that further work in this field will be very promising.

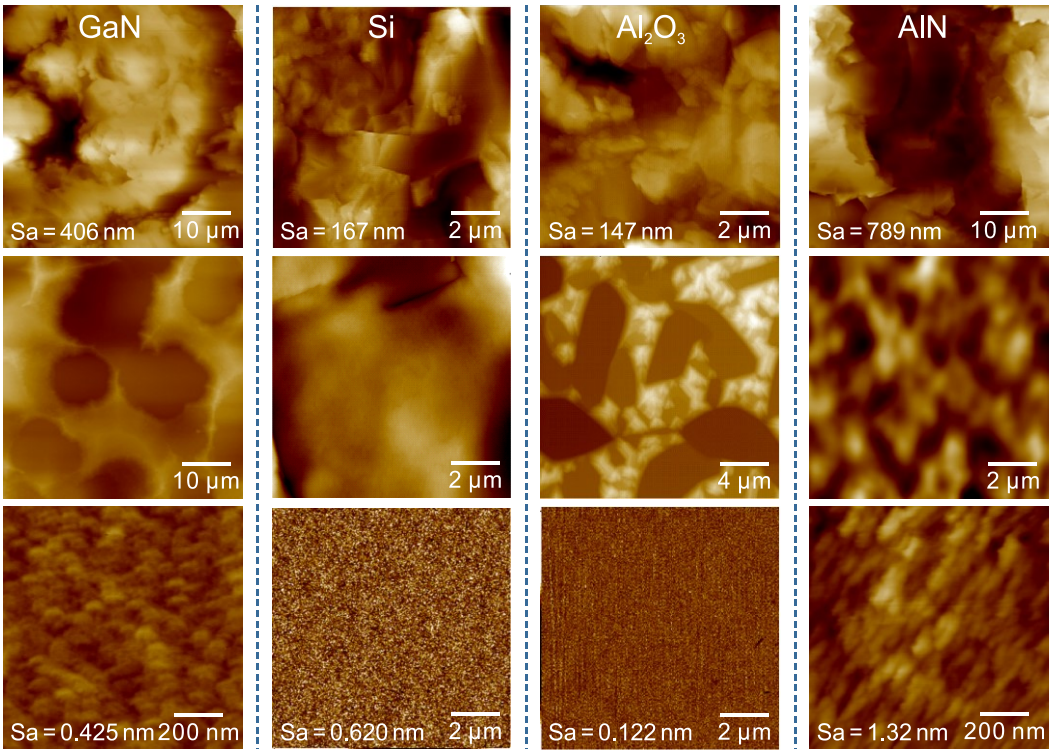


Figure 4.16 The AFM image of GaN, Si, Al_2O_3, and AlN polished by PASE.

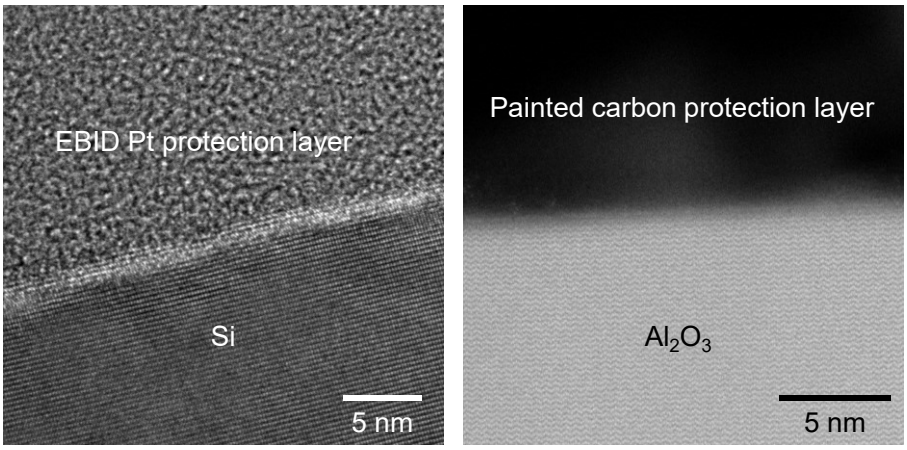


Figure 4.17 The TEM image of the cross-section of (a) Si and (b) Al_2O_3 polished by PASE.

Table 5 The optimized conditions for PASE of different materials

	SiC	Si	Al_2O_3	AlN	GaN
CF_4 rate (SCCM)	30	60	60	30	30
O_2 rate (SCCM)	20	20	0	15	10
Power (W)	>800	>700	800-1000	>800	>700
Temperature (estimated °C)	>1200	>700	>1300	>1300	>1000
Stand-off distance (mm)	20	17-19	24	17	15

4.7 Conclusion

The demonstration of PASE has been conducted based on ICP etching with a heat-insulated sample holder made of alumina foam. Results show that PASE can produce large-scale truly-atomically flat surfaces with ultrafast speed. This method can be a potential solution to the problem of mass-production of atomically flat surfaces of single-crystal materials and foster the applications of third-generation semiconductor materials and the innovation of advanced technologies.

(1) Plasma diagnostics show that the ICP jet contains abundant F and O radicals

which are capable of conducting the etching of SiC. Meanwhile, ICP serves as a heat source that can raise the temperature of the sample over 1400 °C in 60 seconds.

(2) Typical flat-bottom morphology can be observed during PASE, confirming the lateral etching effect. The AFM and TEM results show that PASE can achieve a truly-atomically flat surface. It was noted that the speed of this method is more than 1000 times faster than conventional polishing method and can be used for high throughput production.

(3) The universality of PASE has been demonstrated by various single-crystal materials, which have been achieved with both an atomic roughness and an ultrahigh rate.

Chapter 5

Mechanism of PASE

5.1 Introduction

In the previous chapter, the fast and high precision polishing ability of PASE has been demonstrated, and the flat-bottom morphology, which can confirm the lateral etching effect, has been observed. It was proposed that the lateral etching, which is fundamental to PASE, is originated from the atom-step selective etching. The mechanism for achieving the atom-step selective etching is critical to this research. In this chapter, the mechanism speculation has been given based on experiments of finding the optimized PASE conditions. Subsequently, ab-initio molecular dynamics (AIMD) simulations have been employed to prove the speculated mechanism.

5.2 Mechanism speculation

5.2.1 PASE condition

To speculate the mechanism of PASE, the conditions that can achieve PASE were tested. An interesting phenomenon has been found during the preliminary experiment: there will be different polishing regions on the sample under different stand-off distances. The mechanism for achieving PASE could be related to the distance. Hence, the stand-off distance was the first parameter tested with other operation conditions listed in **Table 6**:

Table 6 The condition for stand-off distance testing.

Parameter	Value
Specimen	10×10 mm n-type sliced 4H-SiC, on-axis
Reaction gas	CF_4 (30 SCCM), O_2 (20 SCCM)
Coolant gas	Argon (18 SLM)
Auxiliary gas	Argon (1.5 SLM)
Duration time	2 min
Stand-off distance	12 mm – 30 mm
Sample holder	Alumina foam 50 mm

Figure 5.1(a) defines the stand-off distance, which is the vertical distance from the ICP nozzle to the workpiece surface. The results are shown in **Figure 5.1(b)**. For the sample etched with a stand-off distance of 12-18 mm, the centre areas remained unpolished, and the surrounding area were polished by PASE. Meanwhile, the unpolished central area shrinks with the increase of stand-off distance. Eventually, the unpolished area disappears in the 20 mm sample, and the whole surface is PASE polished. When the stand-off distance further increases to 22 mm, a rough oxides area appears in the surrounding, and the PASE area shrinks. The PASE area disappears in the 24 mm sample, and a pitting area surrounds the oxide area. As the stand-off distance increases, the oxide area keeps shrinking and eventually, the whole surface was pitting area in the sample etched with 30 mm stand-off distance.

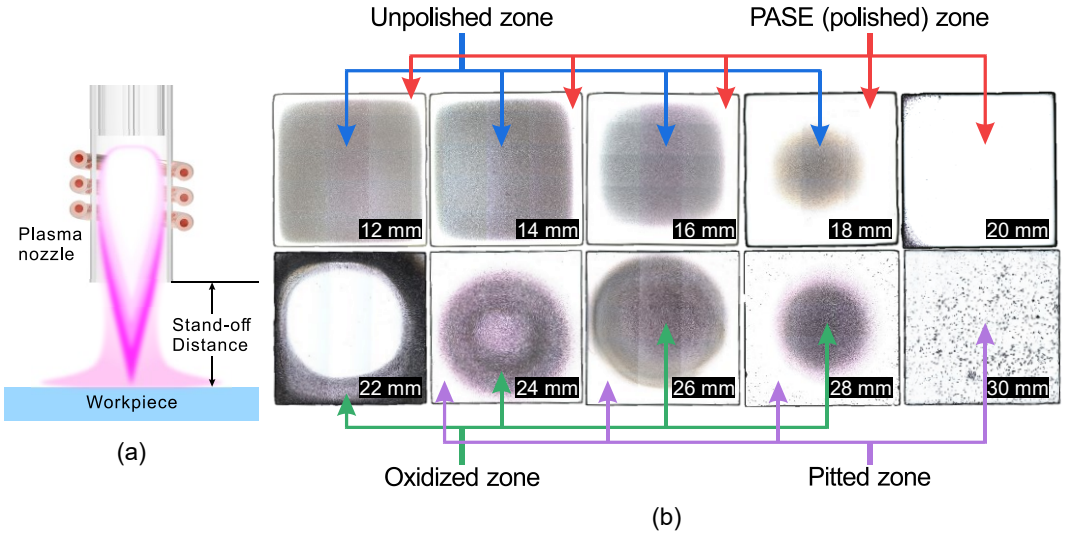


Figure 5.1 (a) the schematic diagram of the stand-off distance, and (b) the SiC sample

etched with different stand-off distances.

A more intuitive schematic diagram is shown in **Figure 5.2**. Different stand-off distances induce different etching area distributions; the optimized PASE condition is 20 mm, where the whole surface of the sample becomes the PASE zone. Multiple factors cause the change of etching morphologies with stand-off distance in **Figure 5.1**: First, an increase of stand-off distance enlarges the gap between the sample and plasma, thus decreasing the sample temperature since plasma is also a heat source. Second, the plasma flow speed could change with increasing stand-off distance. Third, the gas from the ambient atmosphere, mainly the oxygen, mixes with the plasma and changes the reactant composition. The increasing proportion of oxygen generates an oxidized zone. To study the mechanism of PASE, the etching parameters of PASE, including flow rate, temperature, and reactant composition, will be decoupled and investigated separately in the following sections.

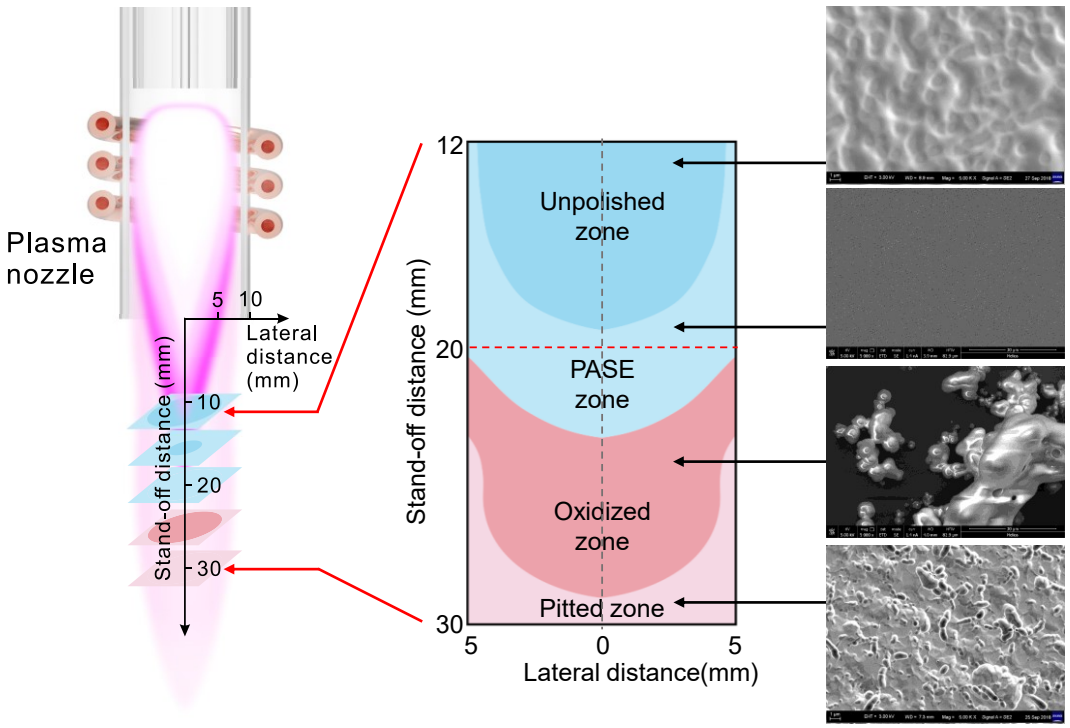


Figure 5.2 The schematic diagram of the etching zone distribution and the SEM image of each zone.

5.2.2 Flow rate

The Flow rate during PASE with different stand-off distances is studied using COMSOL Multiphysics. **Figure 5.3(a)** shows a 3D diagram of the simulated result with a stand-off distance of 20 mm, which is the optimized condition for PASE operation. The velocity distribution is collected from the data collecting zone, which is 1 μm above the sample surface, and the lateral distance from the plasma centre equals 0-6 mm since the flow rate on the sample surface is zero. **Figure 5.3(b)** shows the velocity distribution curve with stand-off distance that varies in the range of 10-30 mm. As the 20 mm sample can be PASE polished globally, the velocity range for the 20 mm sample should be suitable for PASE. However, despite a large overlap of the velocity distribution, PASE did not occur on the sample with 25 mm and 30 mm stand-off distance. The simulated velocity range for the 15 mm sample is fully covered in the range of 20 mm sample, but global PASE did not occur on the 15 mm sample. In addition, the overlap range of the sample with a stand-off distance less than 20 mm is different from the PASE range observed in Figure 5.1. For those samples, the PASE range is the outer ring of the sample, while the velocity overlap zone is the centre. Hence, the velocity is not a sufficient condition for PASE.

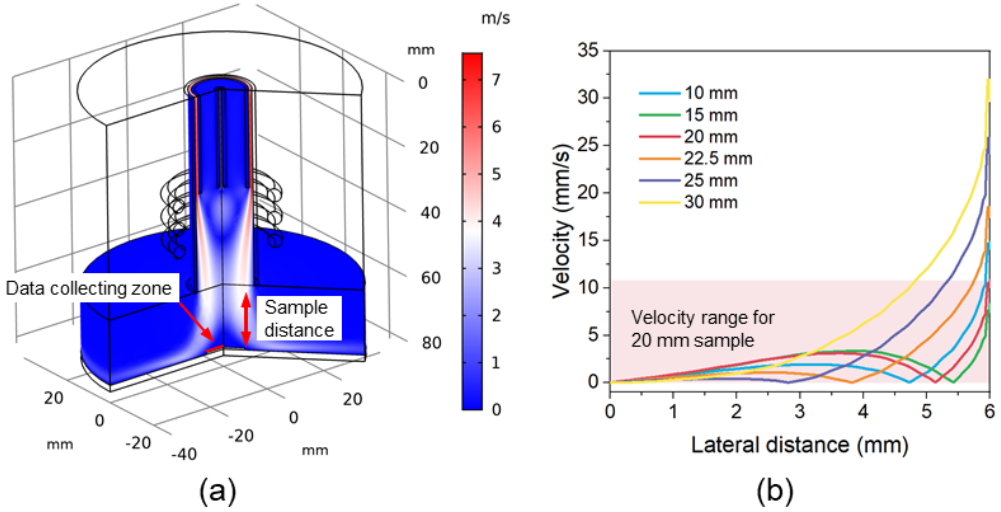


Figure 5.3 (a) The flow velocity simulation of the PASE process with stand-off distance of 20 mm. (b) The velocity distribution alone the data collecting zone with different stand-off distances.

5.2.3 Temperature of the sample

The sample temperature is decoupled and studied experimentally. Four options could lead to the change in temperature: 1. change the stand-off distance; 2. change the gas composition; 3. change the power supply; 4. change the cooling system, which is the sample holder in this study. These four temperature-control strategies have been studied separately in this section.

The stand-off distance has been first applied, as shown in **Figure 5.4**. **Figure 5.4(a)** shows the temperature increasing curve of each stand-off distance, and **Figure 5.4(b)** shows the temperature that each sample reached when etched for 2 mins. The highest temperature is 1688℃ at 12 mm, and the lowest is 1344℃ at 22 mm. The temperature for the samples etched with 24-30 mm is slightly higher than the 22mm sample. As described in **Section 5.1.1**, polish zones were found in the sample etched in a stand-off distance of 12-22 mm, while no polish zone can be found in the sample of 24-30 mm. As the temperature range of the 24-30 mm samples overlaps with the 12-22mm sample and find different etching effect, the temperature is not the sufficient condition to achieve PASE, and the operational temperature range for PASE might be 1300 ℃-1700 ℃

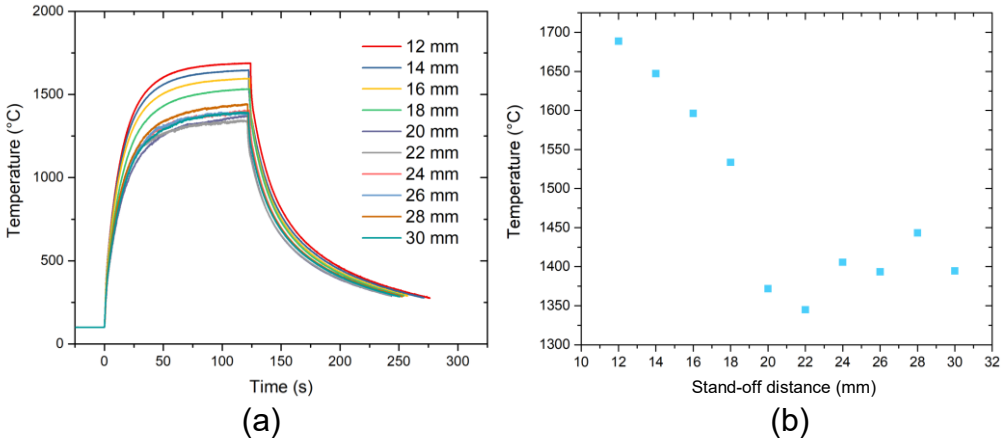


Figure 5.4 (a) the temperature increasing curve of samples etched with different stand-off distances and (b) the temperature they achieved after etched for 2 mins.

As described above, the temperature is not a sufficient condition for PASE.

Thus, changing the gas composition and the power supply is not suitable for studying the influence of temperature, as they will also change the reactant composition. Hence the cooling system has been employed to study the temperature change. The cooling system for the PASE setup can have two options: 1. nozzle cooling for cooling the plasma flow; 2. sample holder cooling for cooling the sample. Cooling the discharge plasma will result in undesirable changes in reactant composition; thus, sample holder cooling was chosen.

As mentioned in **Section 3.3.3**, the change of sample holder with different thermal conductivity will cause a huge temperature change. For instance, the sample on the aluminium sample holder is 315.7℃ while 1737.3℃ on the alumina foam sample holder with other parameters unchanged. The results of the samples etched on those two sample holders are shown in **Figure 5.5**. The sample etched on aluminium, which has a temperature of 300 ~ 400℃, shows a pitting morphology. The pitting is related to the crystal dislocations, which will be discussed in **Chapter 6**. For the sample etched in an alumina foam sample holder with a temperature of over 1400℃, the PASE result is achieved. Hence a high temperature is still needed to achieve PASE. Meanwhile, when the temperature is higher than 1300℃, a further increase in temperature is not very influential to the PASE result.

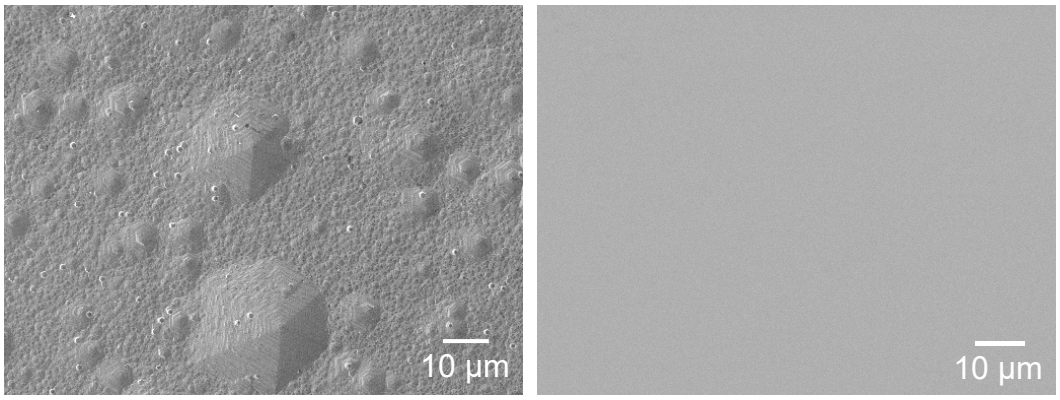


Figure 5.5 The SEM image of PASE etched sample on sample holder made of (a) aluminium (b) alumina foam.

5.2.4 Reactant composition

The reactant composition can be crucial for the PASE effect as described above. Studying the reactant composition can be complex. Considering the ease of operation, the flow rate of CF_4 or O_2 has been kept constant while changing the other composition. Before the investigation, the influence of reactant composition on temperature must be identified. **Figure 5.6** shows the temperature curve of the sample etched by plasma with different reactant compositions. When adding reactant gas into the plasma, the temperature only slightly changes. Moreover, all the temperatures were above 1300℃, which is the suitable temperature for the PASE of SiC. Hence in this study, the influence of temperature change can be neglected.

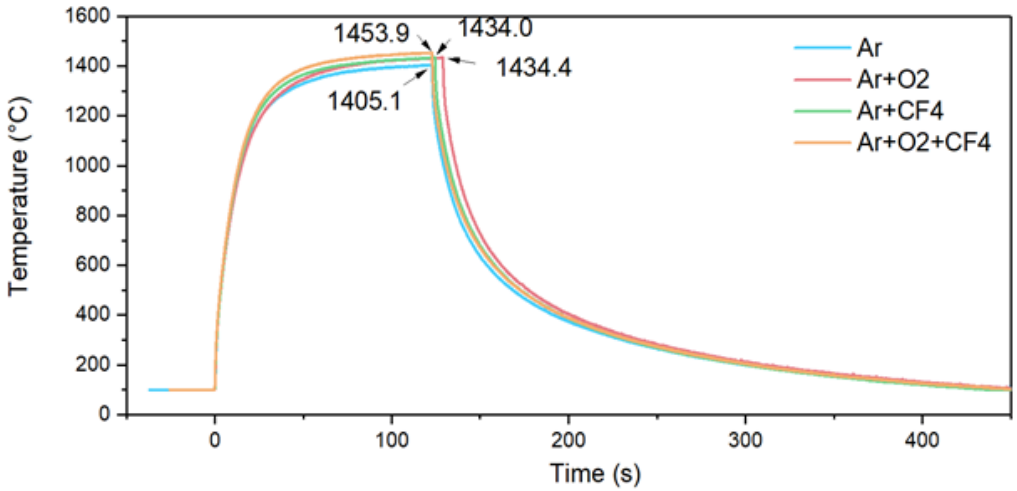


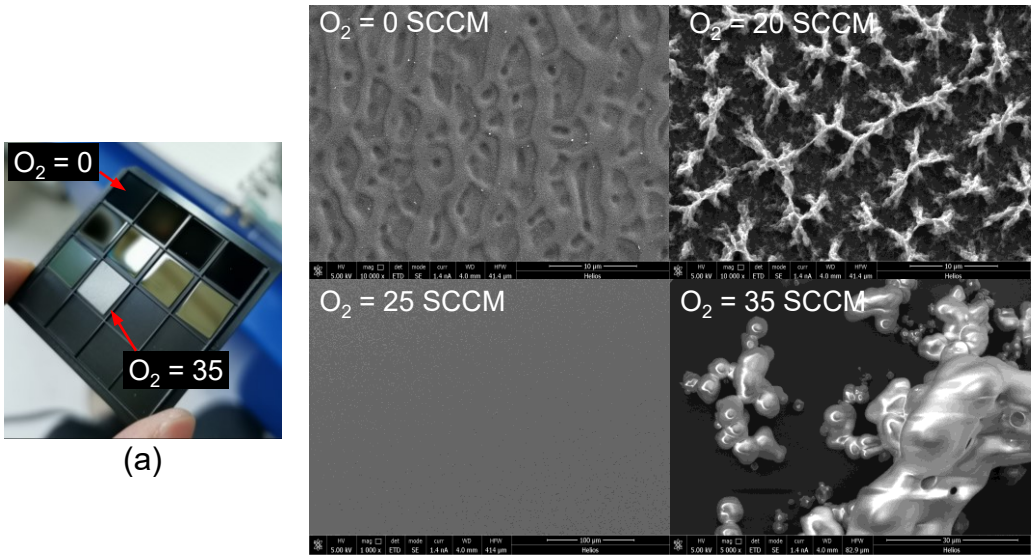
Figure 5.6 The influence of reactant composition on temperature.

During the stand-off distance change experiment described in **Section 5.1.1**, it was discussed that the oxygen concentration in the plasma increases with the increasing stand-off distance. Hence the influence of oxygen has been studied under the conditions listed in **Table 7**.

Table 7 The condition for oxygen testing.

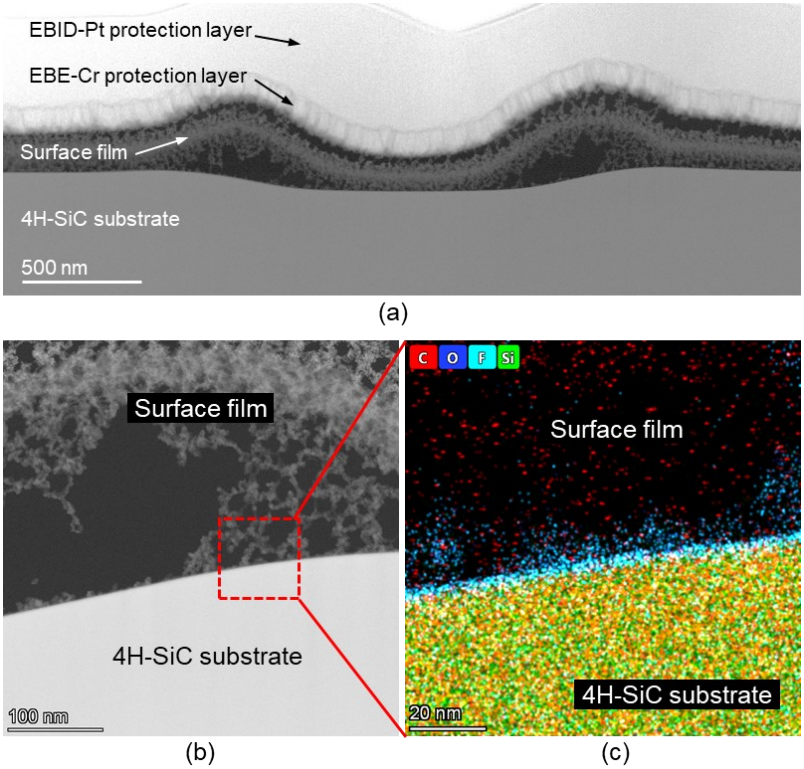
Parameters	Value
Specimen	10×10 mm^2 n-type sliced 4H-SiC, on-axis
Reaction gas (CF_4)	30 SCCM
Reaction gas (O_2)	0-35 SCCM
Coolant gas	Argon (18 SLM)
Auxiliary gas	Argon (1.5 SLM)
Duration time	2 min
stand-off distance	20 mm
Sample holder	Alumina foam 50 mm

The results are shown in **Figure 5.7**. **Figure 5.7(a)** shows the optical image of all the etched samples arranged with oxygen flow increasing from 0 to 35 SCCM. The first four samples, which are etched with oxygen equal to 0, 5, 10, 15 SCCM, respectively, show black colour. The black starts to fade in the sample etched with 20 SCCM oxygen and disappears in the sample etched with oxygen flow higher than 22.5 SCCM. Furthermore, when the oxygen flow rate is higher than 30 SCCM, the sample starts to become covered in white. The SEM images in **Figure 5.5(b)** show four typical morphologies of the etched surface. When there is no oxygen, the sample appears black under the optical camera; the sample surface has been covered in a thick film. The TEM image of the cross-section of this sample is shown in **Figure 5.8(a)**. The surface film is loose and porous, having a thickness of about 100 nm. The loose surface film can absorb light, which leads to the black colour of this sample. The higher magnification image is shown in **Figure 5.8(b)**. The loose file consists of chain structure nanoparticles. **Figure 5.8(c)** shows the EDS image of the interface. It can be seen that the main element of the surface film is carbon. Meanwhile, a very thin (< 10 nm) fluorocarbon layer covers the SiC surface.



(a) (b)

Figure 5.7 (a) The optical image of the sample etched with different oxygen flow rates and (b) SEM image of four typical morphologies.



(a) (b) (c)

Figure 5.8 The TEM image of (a) the cross-section of the sample etched without oxygen, (b) The high magnification image of the film-SiC interface, and (c) The EDS pattern of the interface region in (b).

When the oxygen flow is low, a carbon/fluorocarbon film accumulates on the surface and will hinder the PASE effect. When oxygen flow increases to 20 SCCM, the film partially collapsed and exposed the subsurface. Since the conductivity of

the film and SiC substrate is different, the SEM image shows two high contrast parts, as shown in **Figure 5.7(b)**. When the oxygen flow rate further increases, the carbon film is removed by oxygen. The PASE effect can be achieved, and the surface is well polished. Furthermore, when oxygen flow exceeds the optimized value, the excess oxygen will react with SiC and form SiO_2, which will melt and merge into droplets during etching, as seen in the O_2 = 35 SCCM sample in **Figure 5.7(b)**. Then the sample appears white under the optical camera.

The result suggests that the right proportion of O_2 and CF_4 is needed for achieving PASE. The precise amount of O_2 should remove all carbon/fluorocarbon layers without producing SiO_2. The optimized empirical ratio (CF_4:O_2) for PASE in our experiments ranges from 12:11 to 4:3. The optimized ratio might change when other operation conditions change. For instance, the change of stand-off distance will change the oxygen imported from the ambient atmosphere. Thus, the MFC-controlled oxygen flow rate needs to be modified to make the total oxygen in the plasma remain in the optimized region.

5.2.5 Surface free energy minimization

During the etching of PASE, a spontaneous faceting effect often appears, as shown in **Figure 5.9**. When PASE etches a sliced SiC sample for 8 s, the original hillock will be faceted into a step-terrace structure.

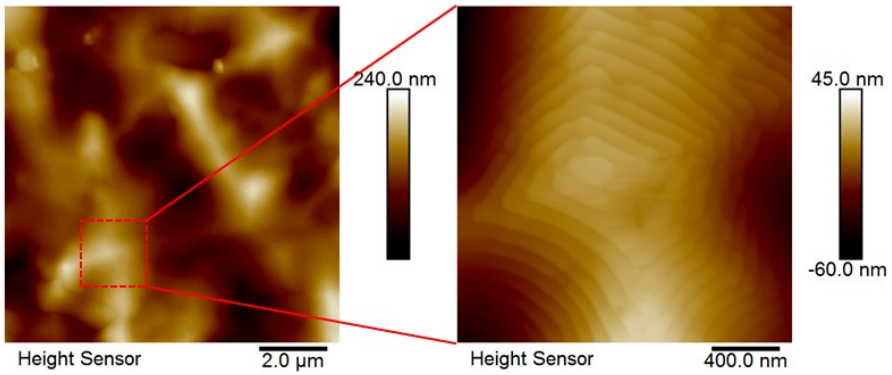


Figure 5.9 The step bunching effect on a sliced SiC sample etched by PASE for 8 s.

A more typical morphology can be observed on the 4° off-cut 4H-SiC sample

etched by PASE for 2 min, as shown in **Figure 5.10**. All the surfaces show ordered microfacets, consisting of two planes, similar to the faceting observed after high-temperature gas etching of SiC [144]. The vicinal angle measure from the AFM profile is about the same as the off-cut angle. The TEM images are viewed from the direction perpendicular to the tilting direction of [11$\bar{2}$0] as shown in **Figure 5.11**. Periodical faceting can be observed clearly, separate the surface into basal planes (0001) and high-index (11$\bar{2}$n) facets with fairly regular periodicity [144]. The typical vicinal angle measured for (11$\bar{2}$n) facets are 8° - 9° under the conducted condition. This phenomenon can be explained in terms of surface free energy and surface elasticity theory [145, 146].

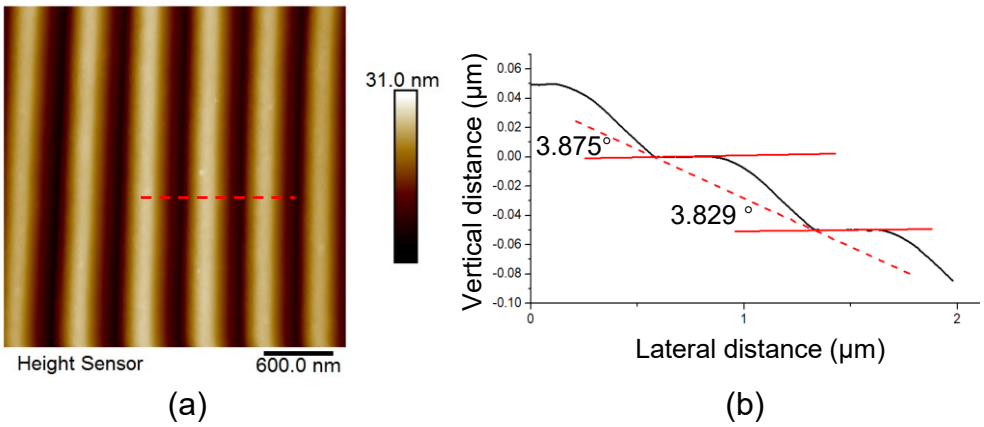


Figure 5.10 The AFM image (tapping amplitude signal) of the 4° off-cut 4H-SiC sample etched by PASE for 2 mins.

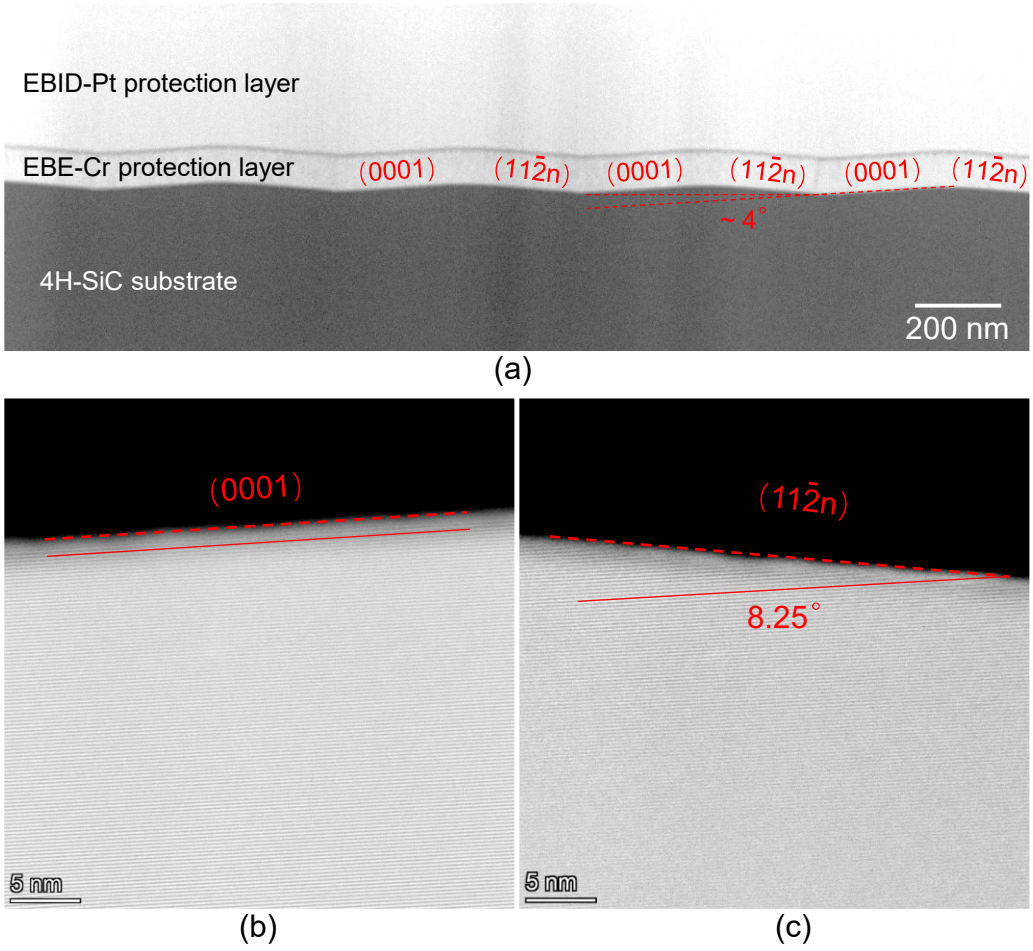


Figure 5.11 (a) The cross-sectional TEM image of 4° off-cut 4H-SiC sample etched by PASE for 2 mins and the HRTEM image of (b) (0001) facet and (c) (11$\bar{2}$n) facet.

The equilibrium surface phase separation theory explains the self-ordering mechanism of the observed micro-faceting on a 4° off-cut 4H-SiC surface [144]. As shown in **Figure 5.12**, the surface free energy curve can be schematic as a function of the vicinal angle between the basal plane (0001) and facet. The surface free energy increases monotonically from (0001) with the vicinal angle increase, as shown by the dashed curve. Another energy minimum point corresponding to an (11$\bar{2}$n) facet can be introduced at 8°-9° as observed by TEM in this study. Notably, this energy minimum point can be affected by experimental conditions like etching temperature. The reduction of surface energy can be induced by the attractive step-step interactions between closely spaced bilayer steps [146]. The dual concave feature of the surface energy curve in **Figure 5.12** can be thus obtained. Since the surface free energy of 4° is higher than (0001) facet, the surface will be separated

into (0001) and (11$\bar{2}$n) facet due to surface free energy minimization. The area ratio of (0001) and (11$\bar{2}$n) facet can be calculated using the lever rule. Hence the width of (0001) and (11$\bar{2}$n) facets are almost the same as observed by AFM and TEM aforementioned.

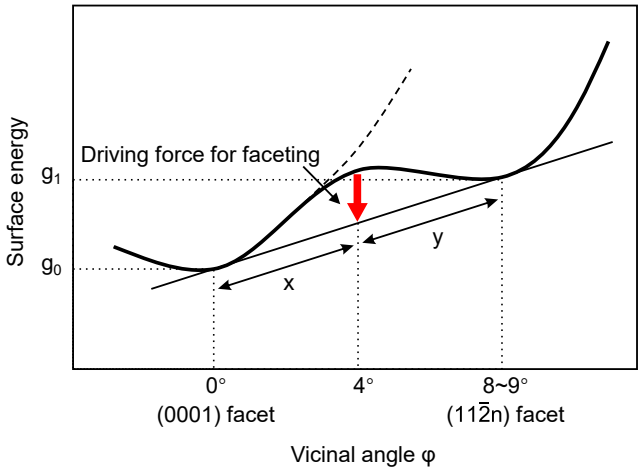


Figure 5.12 The surface free energy curves as a function of vicinal anger.

The mechanism of the ordering of the facet can be explained by the elastic dipole-dipole interaction at the edges of two different facets determined by the ordering periodicity. The periodic arrays of macroscopic step bunches based on the surface free energy can be described by the following equation [145]:

$$E_{total} = E_{terrace} + E_{facet} + E_{edges} + \Delta E_{elastic} \tag{5.1}$$

where E_{total}, $E_{terrace}$, E_{facet}, and E_{edges} are free energies of the terraces, facets, and edges, respectively, $\Delta E_{elastic}$ is the elastic energy due to the discontinuity of the surface stress tensor at the step-edges. E_{total} can be written in the following equation [145]:

$$E_{total} = \gamma_0 + \gamma_1 + \frac{C_1\eta}{D} - \frac{C_2\tau^2}{YD}\ln\left(\frac{D}{a}\right) \tag{5.2}$$

where γ_0 and γ_1 are the surface energy of a flat terrace and step bunch respectively, η is the energy of two edges, D is the period of faceted surface, C_1 and C_2 are geometric factors, τ is the intrinsic surface stress tensor, Y is Young's modulus, and a is the lattice parameter. From **Equation 5.2**, a minimized E_{total} will determine the optimum period of faceting D; hence the step configuration will

be defined.

The aforementioned surface free energy minimization that leads to faceting can also result in a fast-polishing effect for the on-axis 4H-SiC sample. As the (0001) facet has the lowest surface free energy. The comparison of PASE results for 4° off-cut and on-axis and 4H-SiC samples are shown in **Figure 5.13**, and the tapping amplitude signal has been chosen to show the facet more cleanly. The surface of 4° off-cut sample shows ordered facets consisting of (0001) and $(11\bar{2}n)$ planes periodically induced by surface free energy minimization. The on-axis sample shows no facet, and the whole surface is (0001) plane, as the (0001) plane has the lowest surface free energy. Notably, those two samples are directly etched from very rough sliced 4H-SiC samples in just 2 mins. As all the high-index facets, which also form the surface roughness, are removed due to higher surface free energy, the on-axis sample can be polished effectively. It is reasonable to conclude that the surface free energy minimization effect helps polish on-axis 4H-SiC sample.

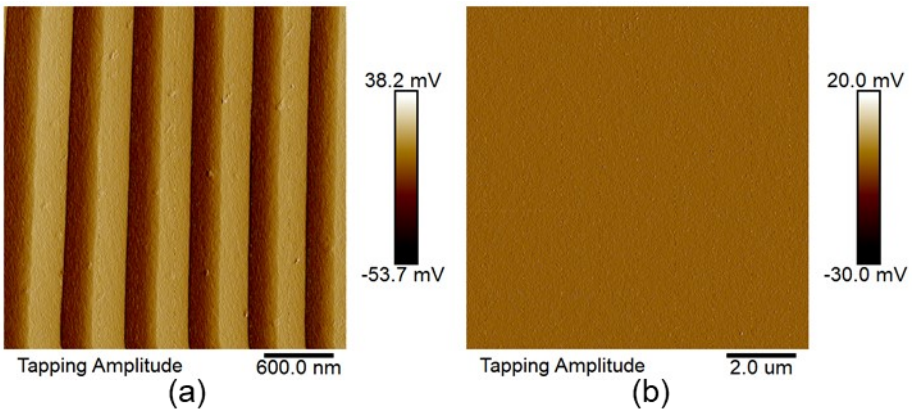


Figure 5.13 The AFM image (tapping amplitude signal) of (a) 4° off-cut and (b) on-axis 4H-SiC samples etched by PASE for 2 min.

5.2.6 Conclusion

In conclusion, the Mechanism for PASE is highly related to the temperature and reactant composition. Meanwhile, the surface free energy minimization helps polish the on-axis samples. In the case of PASE of 4H-SiC in this study, a relatively low temperature (~300℃) will result in a pitting effect. When the temperature is above

1344℃, the PASE effect can be achieved and will not be sensitive to the further increase of temperature. The optimum reactant composition ratio for PASE is CF_4:O_2 = 12:11-4:3. A higher or lower composition ratio will lead to carbon/fluorocarbon film deposition or SiO_2 accumulation. In addition, the surface free energy minimization will cause spontaneous faceting for the vicinal angle sample and help polish the on-axis 4H-SiC samples. The high-index facet that forms the surface roughness will be removed due to higher surface free energy than the basal plane (0001).

5.3 Simulation verification of mechanism

5.3.1 Introduction and methodology

AIMD simulation has been employed to verify the speculation given in **Section 5.1**, as it can simulate chemical reactions with the temperature factor being considered. To facilitate the investigation, the simulation has been divided into two parts: 1. The influence of temperature on atomic selectivity. 2. The role of oxygen in the PASE process.

All calculations were performed using the Density Functional based Tight Binding (DFTB) method implemented in the QUICKSTEP code of the CP2K package. The Perdew–Burke–Ernzerhof density functional, corrected with semi-empirical van der Waals potential energies, was adopted. The plane wave cut-off was set to 400 Ry, and Γ-point mesh for Brillouin zone integration was employed. AIMD simulations were carried by sampling the canonical ensemble employing Nose–Hoover thermostats with a time step of 0.5 fs at a finite temperature. The well-tempered metadynamics-biased ab initio molecular dynamics was performed to explore the free energy surface to identify the minimum free energy pathways, the corresponding activation energies, and the rate-limiting step of the reaction at finite temperatures. The free energy surface was generated by employing a bias factor of 6, Gaussian bias potentials of height 0.05 eV, Gaussian widths of 0.1, and

bias potentials placed every 10 iterations. The stepped 4H-SiC(0001)-$(10 \times 2\sqrt{3})$ surface slab was modeled in which the top surface presents upper and lower terraces with 1×1 periodicity bordered by a single bilayer (SB) step parallel to the $[1\bar{1}00]$ direction. The 4H-SiC(0001)-$(10 \times 2\sqrt{3})$ surface slab deposited with amorphous carbon was constructed by a 4 ps AIMD simulation at 1000 K and 5 ps annealing until the temperature was lower than 10 K. Afterwards, a statics optimization was performed to clean out residual forces. The bottom surface is fixed to the bulk crystallographic positions and terminated by H atoms, whereas the rest of the slab is allowed to relax freely. The slabs were repeated periodically with a vacuum thickness of ~30 Å in the surface normal direction.

To simulate the etching process, etchant atoms (F and O) were added to the 4H-SiC(0001) surface. The initial minimum distance between etchant atoms and the 4H-SiC(0001) surface is greater than 5 Å, and the initial minimum distance of etchant atoms is 4 Å, which guarantees that the atoms are not bonded. Initial velocities of etchant atoms were set at 0.001 a.u. along z-direction of which value is close to the vibration velocities of lattice atoms. When calculating the activation energy of F etching silicon carbide, a single F atom was added to react with the system successively. When simulating the influence of F and O on the morphology of silicon carbide, 16 etchant atoms (F or O) were added to react with the system successively.

5.3.2 Temperature influence of atomic selectivity

Two different substrate models have been built to demonstrate the selectivity towards step-edge atoms, representing terrace and step-edge. The environmental temperature has been set to 300K for low-temperature etching and 1500 K for high-temperature etching. F atoms were used to represent fluorine-containing plasma in this model, considering the ease of simulation. As shown in **Figure 5.13**, the dissociate path of step-edge Si atom (SE-Si) and step terrace Si atom (ST-Si) under

the effect of F plasma is different. The calculated activation energy for SE-Si and ST-Si under 300k is 0.25 eV and 0.53 eV, respectively. And the calculated activation energy for SE-Si and ST-Si under 1500k is 0.23 eV and 0.41 eV, respectively. For both low and high-temperature etching, F plasma shows selectivity towards SE-Si.

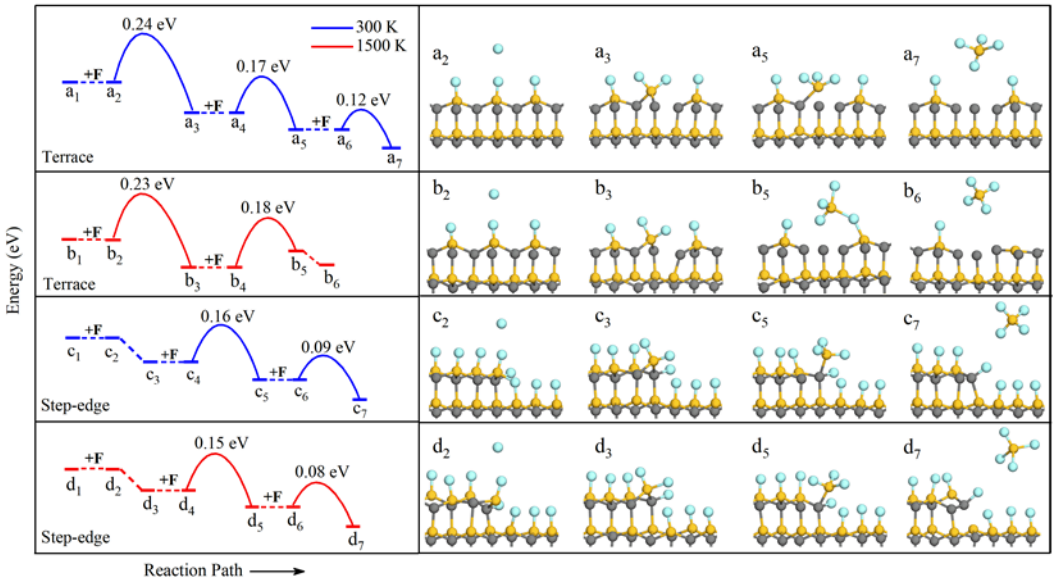


Figure 5.14 The reaction path and activation energy for F etching of SiC in terrace and step-edge at 300K (blue curve) and 1500K (red curve), respectively.

The etching rate can be calculated from the Arrhenius equation [147].

$$k = Ae^{\frac{-Ea}{RT}} \tag{5.3}$$

Where k is the rate constant, T is the absolute temperature (K), A is the pre-exponential factor, which is a constant for each reaction, R is the universal gas constant, and Ea is the activation energy. The etching rate ratio between SE-Si and ST-Si in low and high temperatures can be given by **Equations 5.4** and **5.5**.

$$\frac{k_{SE,\ 300K}}{k_{ST,\ 300K}} = \frac{Ae^{\frac{-Ea_{SE,\ 300K}}{RT}}}{Ae^{\frac{-Ea_{ST,\ 300K}}{RT}}} = e^{\frac{Ea_{ST,\ 300K} - Ea_{SE,\ 300K}}{RT}} \approx 50304.17 \tag{5.4}$$

$$\frac{k_{SE,\ 1500K}}{k_{ST,\ 1500K}} = \frac{Ae^{\frac{-Ea_{SE,\ 1500K}}{RT}}}{Ae^{\frac{-Ea_{ST,\ 1500K}}{RT}}} = e^{\frac{Ea_{ST,\ 1500K} - Ea_{SE,\ 1500K}}{RT}} \approx 4.02 \tag{5.5}$$

Although the etching reaction remains selective towards step-edge (4.02 times higher etching rate at step-edge at 1500K), The selectivity is greatly reduced with the increase of temperature. This result cannot explain the result obtained by the experiment, where higher selectivity emerges under high temperature. To explain this result, the simulation of etching step-edge at 300 K has been extended, and the result is shown in **Figure 5.14**. A step structure on a 4H-SiC substrate has been etched by 6 cycles of F flow. In each cycle, 8 F atoms were injected. It can be observed that after 6 cycles of etching, many amorphous carbons accumulated on the substrate surface, forming the carbon chain and ring structure. This result matches well with the experimental result observed in **Figure 5.7**, where a loose carbon layer formed on the surface after being etched with CF_4 plasma without O_2 addition. This carbon layer will hinder the atom-step structure, and this vanishes the selectivity towards step-edge. Hence, no polishing effect can be observed under this condition.

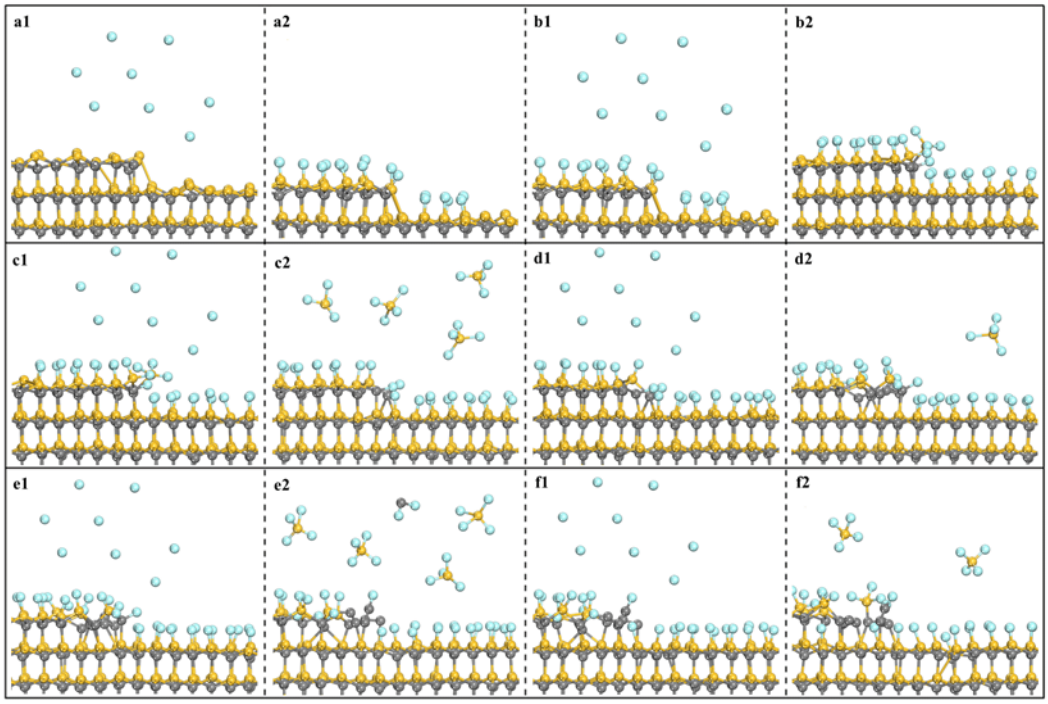


Figure 5.15 The reaction path of F etching of SiC for 6 cycles.

5.3.3 Oxygen

To remove the amorphous carbon layer, O plasma was introduced, and the reaction

process was studied. Here root mean square displacement (RMSD) curve has been employed to study the gas formation and the degree of overall structural change. The RMSD is defined by **Equation 5.6**.

$$RMSD = \sqrt{\frac{1}{N}\sum_{i}^{natom}[(x_i - x_i')^2 + (y_i - y_i')^2 + (z_i - z_i')^2]} \tag{5.6}$$

where N is the number of particles to be averaged, x_i and x_i' is the x coordination of the i_{th} atom in the calculated time position and the reference position, respectively, similar is for y and z. The RMSDs of each etching temperature are shown schematically as a function of time in **Figure 5.15**. It can be observed that 9 CO_X Dissociate at 1500 K, while only 2 CO_X dissociated at 300 K. The ability for oxygen to remove carbon is weak under low temperature and become higher under high temperature[148]. The amount of generated CO_X increases rapidly with temperature. Meanwhile, the carbon removal ability of F has also been tested. At 1500 K, carbon has not dissociated into gas phase compound with the same amount of injecting F atoms, which implies O has a much higher carbon removal ability than F.

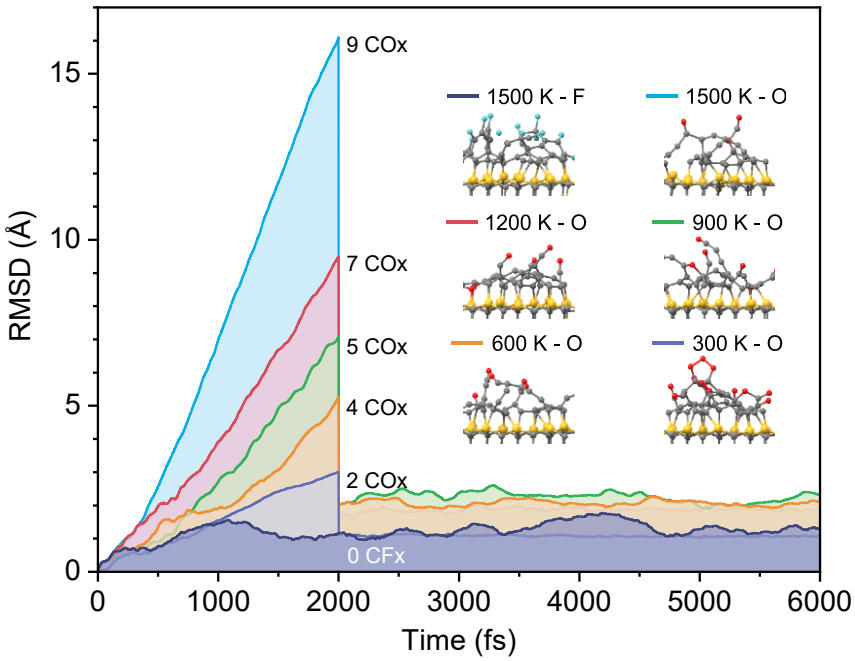


Figure 5.16 The RMSD curve of O and F etching of carbon layer under various temperatures.

When all carbon layer has been removed by oxygen, the exposed SiC surface can be etched by F or O. The circumstances of F etching have been discussed in **Section 5.2.2**. Here, the etching of SiC using O has also been discussed. As shown in **Figure 5.16**, SiC with terrace and step-edge structure has been etched by O at 300 K or 1500 K. At 300 K, the etching shows no visible difference between the terrace and step-edge site, with no gas-phase product generated. However, at 1500 K, the difference starts to emerge. Gas-phase CO has been generated in the step-edge site, while still no gas-phase product from the terrace. This suggests that O has a selectivity towards step-edge under high temperatures. Meanwhile, the absorption of O on the SiC surface will produce a relatively loose Si-O structure, forming active sites that are easy to be etched. And the degree of looseness increased significantly with temperature, as shown by the RMSD curve in **Figure 5.16**. The priority removal of carbon at step-edge will facilitate the selectivity of F towards step-edge. In contrast, the relatively slower dissociation of carbon at the terrace reduces the etching rate of F of ST-Si, further expanding the etching rate differences between SE-Si and ST-Si. Thus, high temperature can promote the carbon removal ability of Oxygen and increase the selectivity towards step-edge.

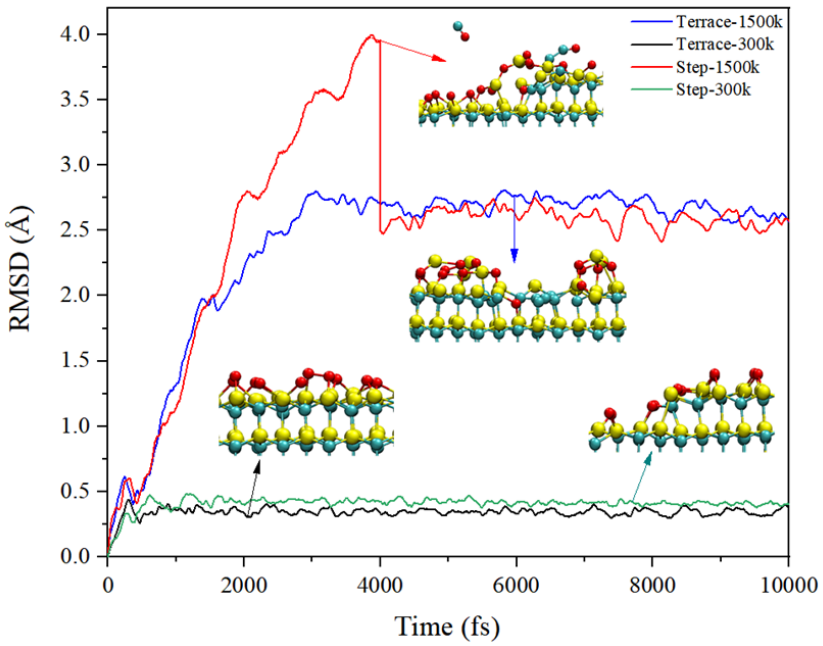


Figure 5.17 The RMSD curve of O etching of SiC in terrace and step-edge at 300K and 1500K, respectively.

5.3.4 Conclusion

To sum up, the combination of F and O plasma at high temperatures can do atom-selective etching of SiC. The F has selectivity towards SE-Si at low and high temperatures, and the selectivity reduces with rising temperature. However, the F etching of SiC will accumulate an amorphous carbon layer at the surface, which will hinder the step-edge and selectivity vanishes. Oxygen can be used to remove carbon and expose the SiC surface behind. The carbon removal ability of O increases rapidly with temperature. Meanwhile, Oxygen shows a selectivity towards step-edge at high temperature, which can further increase the etching rate difference. In addition, O will form a loose Si-O structure on the surface, which can accelerate the etching process. At the macro level, the synergy of F and O could be an effective path for the highly efficient etching of atom steps of SiC. Therefore, the key point to achieve atom-selective etching of SiC is to modulate F and O to an appropriate ratio at high operating temperatures.

5.4 Summary

In this chapter, the mechanism of PASE etching 4H-SiC has been discussed. The optimized experiment condition for PASE has been identified. The related mechanism speculation to achieve PASE has been discussed, and AIMD simulations have helped to prove the mechanism.

(1) In the preliminary experimental study, the PASE condition has been achieved under a certain stand-off distance. The influence conditions were then decoupled into temperature, reactant composition, and flow rate for discussions.

(2) The subsequent experiment suggests that the low temperature will result in pitting. Only a high temperature can realize PASE. When the temperature is above 1300 ℃, the PASE can be achieved but remains insensitive to the further rise in temperature. The optimum reactant composition ratio (CF_4:O_2) for PASE

is in the range of 12:11 to 4:3. A higher or lower composition ratio will lead to carbon/fluorocarbon film deposition or SiO2 accumulation, respectively.

(3) In addition, the surface free energy minimization will cause spontaneous faceting for the vicinal angle sample and help polish the on-axis 4H-SiC samples. The high-index facet that forms the surface roughness will be removed due to higher surface free energy than the basal plane (0001).

(4) Simulation results show that F indicates selectivity towards step-edge at all temperatures during the etching process. However, the selectivity decreases with temperature increase for F etching.

(5) The etching of SiC using F will cause amorphous carbon accumulation. This carbon layer will hinder the step-edge and vanish the selectivity. And F is not capable of removing the carbon layer. This matches well with the experimental results observed when the oxygen addition is low.

(6) The introduction of oxygen can remove the carbon layer, and the removal ability increases greatly as the temperature increases. Meanwhile, oxygen shows selectivity towards step-edge at high temperatures and can produce a loose Si-O structure, facilitating the etching and further increasing the overall selectivity for the F/O mixture plasma towards step-edge.

(7) For F/O mixture plasma, oxygen is the key element that needs high temperature to promote selectivity etching. High temperature can increase the removal rate of amorphous carbon by oxygen and increase the selectivity towards step-edge for oxygen. At high temperatures, F and O selectivity etch Si and C, respectively. The synergy of F and O is the key to achieving a highly efficient etching of step-edge of SiC. Hence, high temperature and appropriate F/O ratio are the two indispensable conditions to achieve PASE.

Chapter 6

Dislocation detection and elimination

6.1 Introduction

As mentioned in **Section 5.1.3**, the etching of SiC at a relatively low temperature (300~400 ℃) will lead to a pitting morphology, which is tightly related to the crystal dislocation. A rational presumption is proposed that the selectivity of PASE could be modulated toward dislocations or atoms step-edges by the temperature. Furthermore, the modulated version of PASE with selectivity toward dislocation (PASE-D) could be a promising method for the dislocation detection of SiC and other single-crystal materials. In this chapter, the dislocation revealing the ability of PASE-D is demonstrated. Low-temperature etching with CCP and ICP on the cooling sample holder is conducted. A comparison with the conventional KOH etching method is presented. The mechanism speculation is based on the study of dislocation pits angle change. The elimination of the dislocation based on the speculated mechanism has been tested, and the PASE effect has been attempted to directly achieved by molten KOH etching.

6.2 Detection of dislocation [149]

To reveal dislocations in SiC wafers, conventionally, the molten KOH etching method has been widely used. However, when highly doped sites exist on the wafer, the molten KOH etching method is not applicable owing to the enhanced isotropic electrochemical etching phenomenon. In this study, plasma etching is first applied to reveal dislocations in a 4H-SiC wafer with both highly doped and lightly doped

areas. The mechanisms of dislocation revelation by dry etching have been theoretically analyzed, and it has been revealed that the dislocation revelation ability of dry etching is highly related to the temperature of the etching process. The results demonstrate that PASE-D can maintain its effectiveness for dislocation revelation of SiC wafers regardless of the doping concentrations. This work offers an alternative approach to indiscriminately and accurately reveal dislocations in SiC wafers

6.2.1 Conventional KOH etching

4H-SiC samples with low doping concentration (10^{18} cm^{-3}) and high doping concentration (> 10^{19} cm^{-3}) have been etched using this method, and the results are shown in **Figure 6.1**. After etching, the low doping area (**Figure 6.1(a)**) is covered with etching pits, and three kinds of dislocations can be identified from the shape. TSDs (threading screw dislocations) and TEDs (threading edge dislocations) are revealed as hexagonal etching pits with relatively bigger and small sizes [150]. The etching pits caused by BPDs (basal plane dislocations) usually form seashell shape instead [151]. Some etching pits originated from TEDs have lost their hexagonal shape and turned to be oval. It means that even in the relatively low doping area, isotropic electrochemical etching is still significant [152]. This result also proves that the conventional molten KOH etching method is susceptible to the doping concentration of the SiC wafer. However, only a few shallow etching pits could be found for the high doping area (**Figure 6.1(b)**). Moreover, it is virtually impossible to recognize the dislocation type from the shape of the etching pits. Based on these results, it is concluded that using the conventional molten KOH etching method to reveal dislocations for highly doped n-type 4H-SiC is impractical.

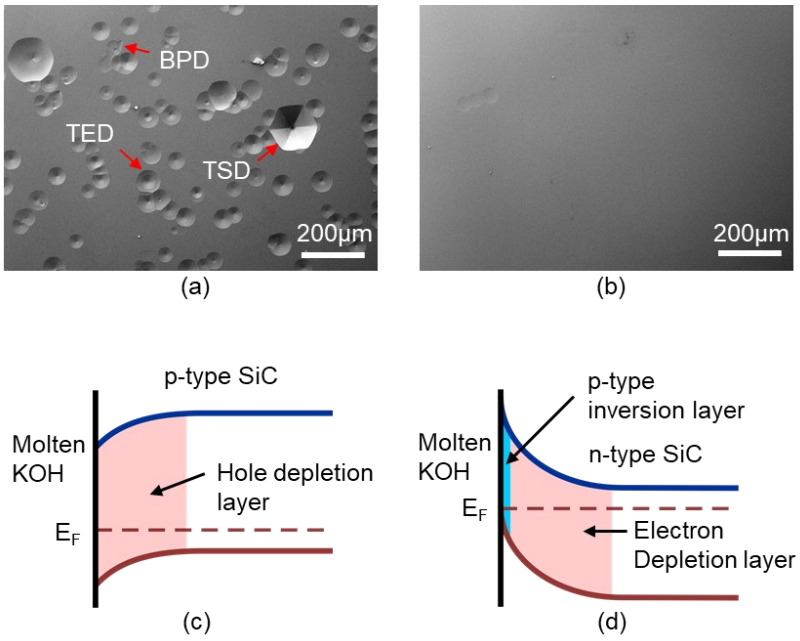


Figure 6.1 (a, b) SEM images of the molten KOH etched surface of low doping SiC and high doping SiC. (c, d) Band structure schematics of 4H-SiC/molten KOH interface for p-type SiC and high doping n-type. [149]

The mechanism of this phenomenon has been discussed by Gao *et al.* in detail [153]. Molten KOH etching of SiC consists of two parallel reactions: chemical reaction and electrochemical reaction, although there is no external bias. The chemical reaction will preferentially attack the defect spot due to energy relaxation of those places, thus it is selective to dislocations. While electrochemical etching, in this case, is a kind of anode oxidation reaction and mainly depends on the availability of holes which shows no selectiveness to dislocations [154]. The competition between a chemical reaction and an electrochemical reaction defines the final morphology of the etched surface. Gao *et al*. [153] suggest that when SiC is contacting with molten KOH, band bending happens at the solid-liquid interface, analogous to the band bending in the SiC-HF interface observed by J. S. Shor *et al.* [155]. For p-type SiC, the energy band bends downward (**Figure 6.1(c)**), forming a hole depletion layer. This layer contains no mobile holes and acts like a barrier that prevents charge exchange, therefore, hinders electrochemical reaction. The dominant chemical reaction will preferentially attack the defect sites; thus, dislocation revelation works well. In contrast, for sufficiently high doping n-type

SiC (**Figure 6.1(d)**), the undue band bending will cause a p-type inversion layer at the interface, which provides substantial holes as a free carrier [156]. The electrochemical reactions will then become dominant due to the abundant holes. Meanwhile, as the electrochemical reaction depends entirely on the availability of holes, the etching of the p-type inversion layer will be uniform regardless of the presence of defects. This leads to the failure of conventional KOH method when conduct dislocation revelation over high doping n-type SiC substrates.

6.2.2 CCP etching

An etching process without electrochemical reaction must be found to overcome the problem existing in the conventional molten KOH etching method and find a new approach to realize doping-density-independent dislocation revelation. One solution is choosing a kind of etching process without the solid-liquid interface to prevent the band bending due to contact potential [157]. As a typical dry etching process, plasma etching does not form the solid-liquid interface [158]; thus, electrochemical reactions, which invalidate the molten KOH etching process, will not happen. Therefore, plasma dry etching is supposed to effectively reveal the dislocations in SiC wafers accurately. CCP is one of the most commonly used plasma sources for semiconductor applications owing to its good stability and controllability [159]. With the capability to ignite discharge under atmospheric pressure, CCP can operate without an expensive vacuum system [160]. **Figure 6.2(a)** shows the schematic of the CCP device used in this study, and **Figure 6.2(b)** is the optical photo of the CCP jet. The chemical reactions occurring in the CCP etching process can be expressed in **Equation 4.1**: According to this equation, fluorine radicals and oxygen radicals are involved in the etching of SiC. Here, CF_4 has been chosen as the fluorine source and O_2 as the oxygen source with respective flow rates of 20 SCCM and 10 SCCM. OES has been employed to investigate the radicals in plasma, and the typical OES spectra of the CCP jet at 50 W is shown in **Figure 6.2(c)**. Helium peaks (501, 587, 667, 706, 728 nm) mainly formed due to

the collision of energetic electrons with helium atoms, can be seen clearly [161, 162]. The oxygen atom emission at 777 nm and 844 nm are observable [141]. The nitrogen peaks (316, 337, 357, 380 nm), which come from the participation of ambient air during plasma discharge, are also visible for the plasma jet [141, 162]. The CF_X continuum (ranges 280–400 nm) and CF_3 continuum (550–650 nm) are well pronounced [163]. Emissions from fluorine atoms (600–750 nm) are not very striking due to their extremely short lives at atmospheric pressure [138].

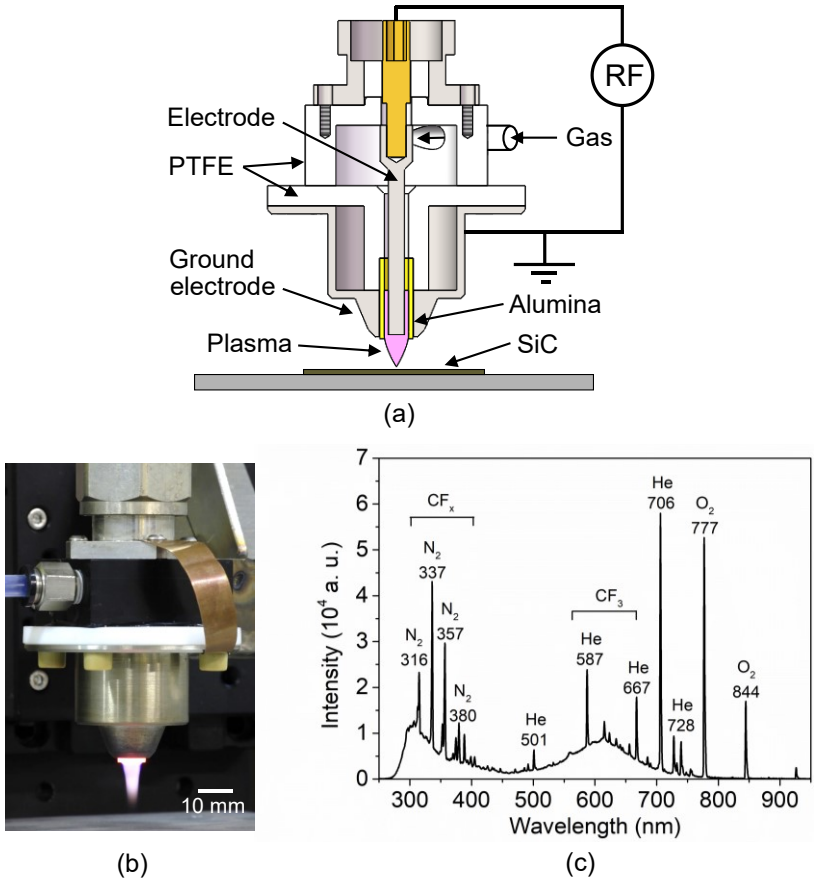


Figure 6.2 (a) Schematic diagram of the experimental setup for CCP jet etching. (b) optical photo of the CCP jet. (c) OES spectra of the CCP jet. [149]

This CCP jet has been employed to etch the Si-face of 4H-SiC. **Figure 6.3(a)** shows the raw surface before the treatment. A clear step-terrace structure suggests that the surface is well polished and not covered by other impurities. The step-terrace structure indicating the surface molecular fluctuation can also be seen in the surface cross-sectional profile (**Figure 6.3(c)**). However, the step-terrace structure

disappeared after etching, and the surface became visually uniform, covered with randomly distributed small pits or valleys (**Figure 6.3(b)**). From the cross-sectional profile (**Figure 6.3(d)**), it can be observed that the etching randomly occurred. The disappearance of the step-terrace structure shows the etching was non-selectivity to the step-edges. The visually uniform surface implies it also has no preference for dislocation sites. These results suggest that roughly isotropic etching has been performed using CCP. The isotropic properties of CCP could be originated from the low reaction activity, low reactant concentration, and high deposition rate of by-products due to the low temperature and power. Hence, it is not capable of revealing dislocations.

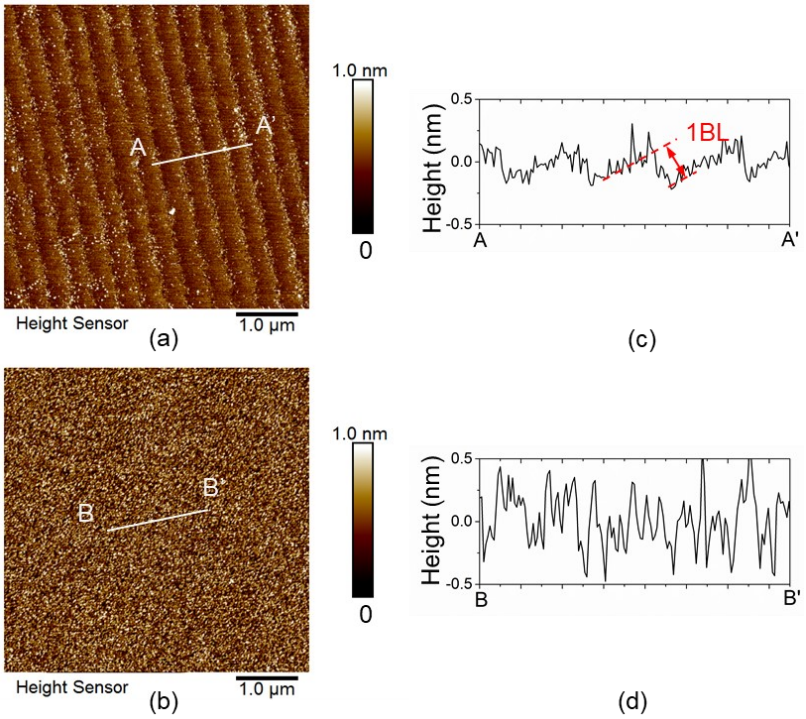


Figure 6.3 (a, b) AFM images of the Si face of the 4H-SiC sample (a) before and (b) after CCP etching. (c, d) Cross-sectional profiles along A-A' and B-B', respectively. [149]

6.2.3 Mechanism speculation

To find out why CCP etching only got a uniform surface without pronounced etching pits for dislocations, the temperature of the sample during the CCP etching process has been measured. As shown in **Figure 6.4**, the temperature of the SiC

surface was slightly higher than the atmosphere temperature. The average substrate temperature was around 40 °C, and the maximum temperature was about 70 °C. The low temperature has been considered the reason for the isotropic etching shown in **Figure 6.3(e)**, and the mechanism is as follows.

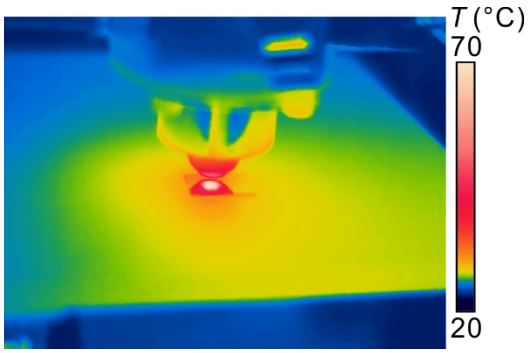


Figure 6.4 The thermal image of the substrate during CCP etching [149]

Figure 6.5(a) is the schematic of the cross-section of a 4H-SiC sample with a threading dislocation line. The formation of etching pits is considered to be originated from the difference of etching rates between perfect crystalline surface and dislocation sites [164]. We assume the etching rate for perfect crystalline Si-face of 4H-SiC to be v_p, and the etching rate for the dislocation sites to be v_d. Etching rate v_p is governed by Arrhenius equation [147, 165]:

$$v_p = n_F A exp\left\{\frac{-Ea}{RT}\right\} \tag{6.1}$$

where A is the pre-exponential factor, which is a constant for the specific reaction, n_F is the concentration of fluorine radicals on the surface. Ea is the activation energy for the chemical reaction, R is the universal gas constant, and T is the absolute temperature of the sample surface. At the dislocation sites, stress-energy that promotes the etching process exists [164]. Thus, the activation energy of the dislocation sites should be slightly smaller than that of the perfect crystal surface, and the difference is expressed as ΔE. Then the expression of v_d is given by **Equation 6.2**:

$$v_d = n_F A exp\left\{\frac{-(Ea - \Delta E)}{RT}\right\} \tag{6.2}$$

Then, the pitting speed, which is also the relative etching rate between v_d and v_p can be expressed by **Equation 6.3**:

$$v_{\text{pits}} = v_d - v_p = n_F A exp\left\{\frac{-Ea}{RT}\right\}\left\{exp\left\{\frac{\Delta E}{RT}\right\} - 1\right\} \tag{6.3}$$

As the dislocations in SiC are mainly linear, $\Delta E\ (RT)^{-1}$ should be a small value[166]. Thus, **Equation 6.3** can be written into this formula:

$$\begin{aligned} v_{\text{pits}} &= n_F A exp\left\{\frac{-Ea}{RT}\right\}\left\{exp\left\{\frac{\Delta E}{RT}\right\} - 1\right\} \\ &\cong n_F A exp\left\{\frac{-Ea}{RT}\right\}\frac{\Delta E}{RT} \end{aligned} \tag{6.4}$$

In **Equation 6.4**, n_F, A, and ΔE are all considered constants in the dry etching process, and they will not change with temperature. Thus, rest of the equation needs to be considered only. Here, V has been used as the temperature-dependent part of **Equation 6.4**.

$$V = \frac{v_{\text{pits}}}{n_F A \Delta E} = \exp\left(\frac{-Ea}{RT}\right)\frac{1}{RT} \tag{6.5}$$

Using the activation energy calculated by Sano *et al*. [167], the V can be plotted as **Figure 6.5(d)**. It has been demonstrated from the plot that in the temperature range of 300-1000 K, the pitting speed for dislocation sites will increase significantly with the temperature. At a low temperature around 300 K, as shown in **Figure 6.5(b)**, the difference between v_d and v_p is in significant. Thus, v_{pits} is very small. Both perfect crystalline surface and dislocation sites were etched almost uniformly. Thus no etching pits standing for dislocations could be formed. However, at a medium temperature of around 700 K, v_{pits} can be more than 1000 times higher than that at low temperature. Thus, dislocations could be revealed efficiently, as demonstrated in **Figure 6.5(c)**.

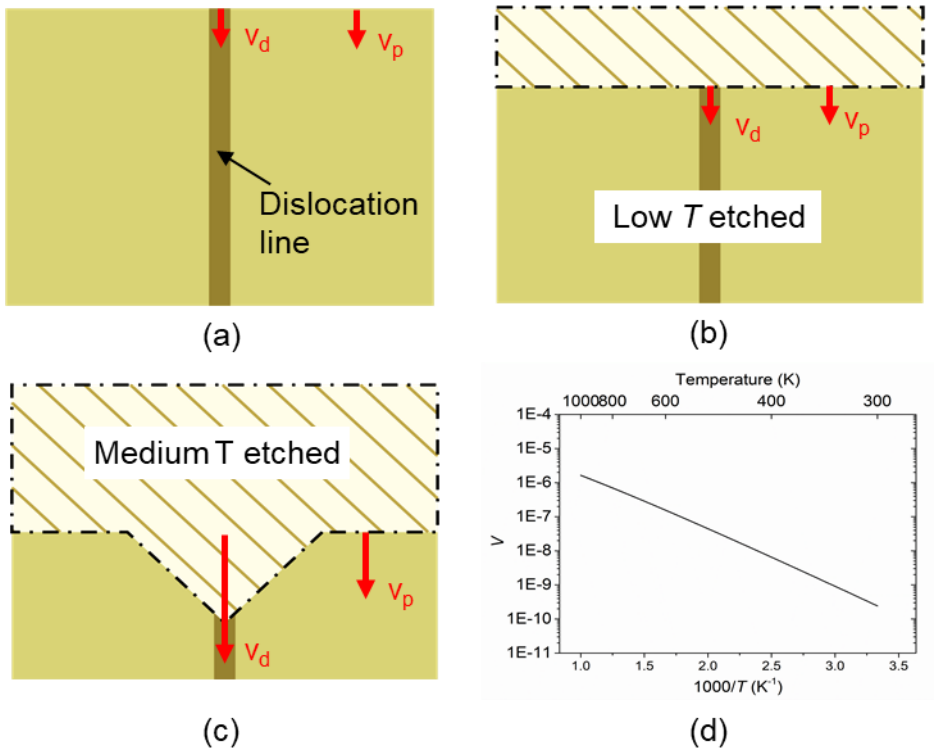


Figure 6.5 (a)-(c) Schematic of 4H-SiC with a threading dislocation line (a) before etching, (b) after low-temperature etching, and (c) medium temperature etching; (d) the Arrhenius style plot of V-Temperature. [149]

6.2.4 ICP etching

According to the dislocation revelation mechanisms discussed above, dry etching cannot reveal dislocation; a medium-high etching temperature is indispensable. Atmospheric pressure ICP has generally been possessing both higher temperature (5000–7000 K) and higher radical density (10^{13}–10^{17} cm^{-3}) [168]. Meanwhile, ICP-based PASE can have a modulated etching temperature by changing the sample holder as presented in **Section 3.3.3**. As mentioned in **Section 5.1.3**, PASE on an aluminium sample holder with a medium temperature of ~ 400 °C, will reveal hexagonal etching pits on the substrate surface, similar to the hexagonal pits observed in **Figure 6.1**. It can be proposed that the changing temperature in PASE from high (>1300°C) to medium (~ 400°C) results in a shift of selectively etching site from atom step-edges to dislocations. The modulated version of PASE with selectivity towards dislocation is named PASE-D.

Figure 6.6(a) shows the schematic of the PASE-D setup used in this study. The thermal image (**Figure 6.6(b)**) of the SiC sample during PASE-D shows the average surface temperature of the sample is 350°C, and the maximum temperature is 458.7°C. Therefore, the pitting speed to reveal dislocations could be more than 1000 times higher than operating at room temperature according to **Figure 6.5(d)**, suggesting that the PASE-D should be applicable for dislocation revelation of SiC wafers.

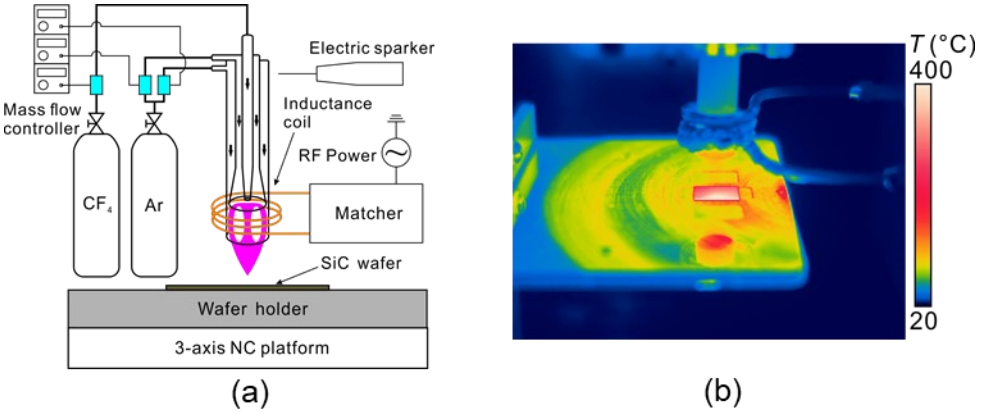


Figure 6.6 (a) Schematic diagram of the experimental setup for PASE-D.(b) thermal image of the substrate during PASE-D. [149]

PASE-D has been performed on the Si-face of a 4H-SiC wafer, and the results are shown in **Figure 6.7**. **Figure 6.7(a)** shows the SEM image of the etched surface; many hexagonal etching pits were formed as forecasted. Those hexagonal etching pits can be mainly divided into two groups. The larger hexagonal etching pits stand for micropipes and TSDs, while the smaller ones stand for TEDs. A close-up view of a micropipe originated etching pit is shown in **Figure 6.7(b)**. It is a bottomless hexagonal pit as most micropipes are deep and threading through the whole wafer [169]. **Figure 6.7(c)** shows an etching pit that originated from a TSD. It is much bigger than etching pits originated from TEDs, as shown in **Figure 6.7(d)**. The size difference of etching pits originates from the difference in pitting speeds for each type of dislocations, which is further determined by the strain energy at the dislocation sites. The strain energy of dislocations is proportional to the square of

its burger vector [164]. No seashell-shaped etching pits corresponding to BPDs have been observed in this sample. This has been considered owing to the dislocation conversion effect [170]. **Figure 6.7(e)** shows the surface morphology of the pit-free area of the wafer. This surface is supposed to be the perfect crystalline surface without pronounced etching pits standing for dislocations. However, it is still covered by visually uniform small etching pits. It is suggested to result from preferential etching caused by thermal noise. According to the Arrhenius equation, as the average temperature of this sample is very high during PASE-D, a small random heat fluctuation will cause huge difference in etching rate [147]. Thus, countless uniform small etching pits were formed on the surface. These results prove that the proposal to reveal dislocations in SiC using PASE-D is effective.

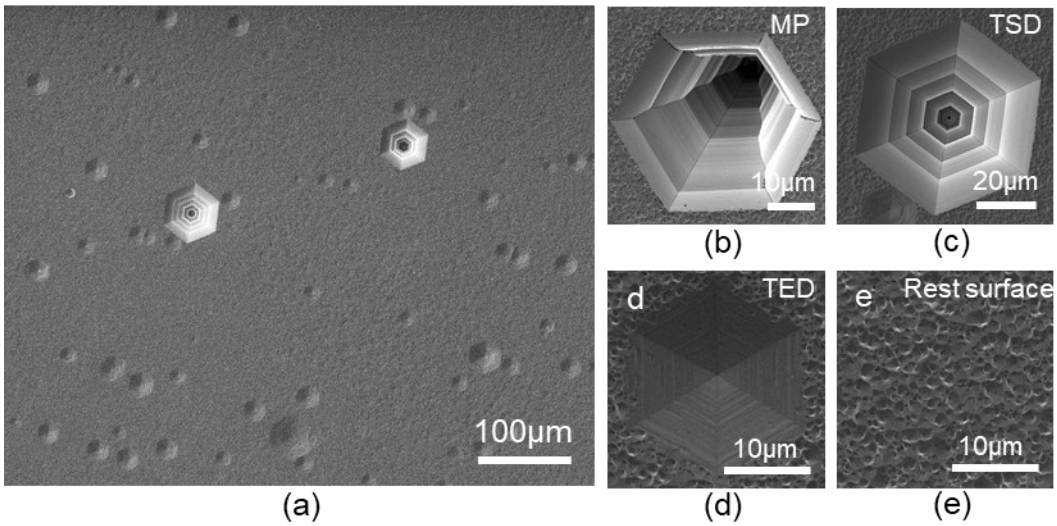


Figure 6.7 (a) SEM image of the PASE-D etched surface of SiC and the close-up SEM image of (b) MP; (c) TSD; (d) TED and (e) the rest surface. [149]

6.2.5 Comparative study between conventional molten KOH etching and PASE-D

Comparative experiments were carried out to compare the dislocation revelation ability of the conventional molten KOH etching method and the PASE-D method for 4H-SiC with different doping concentrations. To ensure the dislocation density

for the high doping sample and low doping sample are similar, a SiC wafer containing both low doping area and high doping area has been used (**Figure 6.8(a)**). This wafer was cut into two SiC sheets, approximately 10 mm×20 mm in size. And both sheets contain low doping area and high doping area with almost the same proportion as marked. One SiC sheet was treated with the conventional method (marked no. 1) and the other with the ICP etching method (marked no. 2), and then the results were discussed. **Figure 6.8(b)** shows that the left part is the sample treated with the conventional molten KOH etching method. The surface morphologies are obviously different between the low doping area and high doping area, which has also been proved by the SEM observation covering the boundary area as shown in **Figure 6.8(c)**. The low doping area is covered by uniform distributed etching pits, with size separated into two groups. This implies that dislocations are well detected in this area. However, only a few etching pits can be recognized for the high doping area. Most areas remain a specular surface, suggesting isotropic etching has been dominant, and dislocations have not been revealed efficiently. For the right part in Figure 6b, which is the sample treated with the PASE-D method, the whole SiC sheet is visually uniform. Both high and low doping areas are covered with etching pits, as demonstrated by the SEM image shown in **Figure 6.8(d)**. With the border being marked using a marked line, no significant difference can be found across the border.

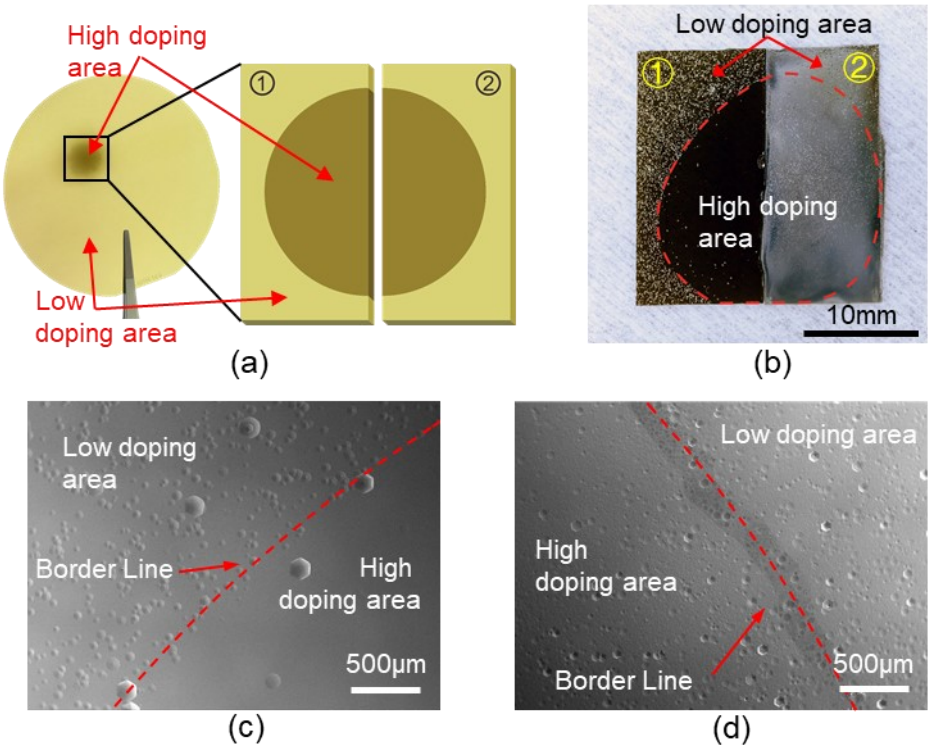


Figure 6.8 (a) Optical photo of the SiC wafer used (left) and the schematic of the two samples cut off from that wafer (right). (b) Optical photo of the samples after conventional molten KOH etching and PASE-D, respectively. (c, d) SEM images for the boundary area between low doping area and high doping area of SiC etched by (c) conventional method and (d) PASE-D method. [149]

To further evaluate the dislocation revelation results, EPD (etching pits density) has been employed to show the density of dislocations exposed at the etched surfaces. **Figure 6.9(a)** shows the size distribution of the etching pits on a SiC sample etched by molten KOH. The number of etching pits with different sizes has been quite different for the lightly doped and highly doped areas. The number of etching pits counted for the low doping area was 419, while only 28 etching pits were observed for the high doping area. The EPD for the low doping area is 9.3×10^3 cm^{-2}, which is slightly lower than the EPD measured by ICP etching and the typical dislocation density of the 4H-SiC substrate, which is 10^4 cm^{-2}. It means that even for the relatively lightly doped area, the measured EPD using the molten KOH etching method is still questionable. As for the EPD measured on the highly doped area, it is only 6.2×10^2 cm^{-2}, which is far below the actual value. The size distribution of etching pits on SiC after PASE-D has been shown in **Figure 6.9(b)**.

The number of etching pits for the two areas on this sample has been very close. 680 etching pits were found on the low doping area, and 789 etching pits were found on the high doping area. EPDs for the low and high doping areas are 1.5×10^4 cm^{-2} and 1.7×10^4 $cm^{-2,}$ respectively, which are very close to the specific value. These results demonstrate that PASE-D is an effective and accurate approach for dislocation revelation for low and high doping SiC.

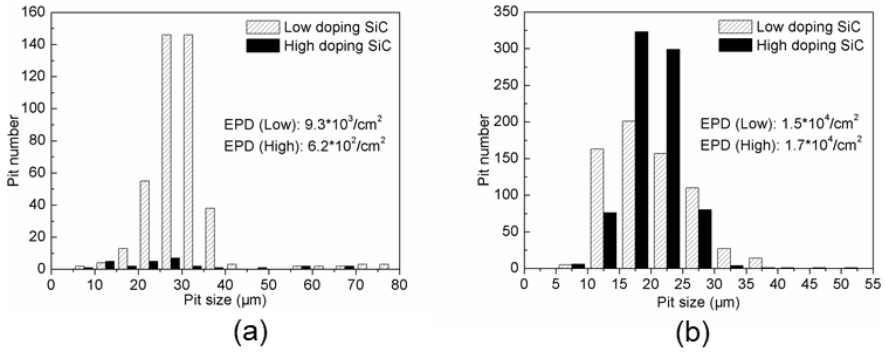


Figure 6.9 Size distribution of etching pits of the low and high doping areas for SiC samples processed by (e) molten KOH etching and (f) PASE-D. [149]

6.2.6 Conclusion

In summary, an indiscriminate and accurate dislocation revelation of single-crystal SiC can be realized using PASE-D. The conventional molten KOH etching method failed to reveal the dislocations in the highly doped wafer area due to the isotropic electrochemical etching phenomenon. To avert the electrochemical etching problem, plasma dry etching has been utilized. Based on CCP etching results and plasma etching kinetics analysis, it has been proved that dislocation revelation in plasma dry etching is highly related to the process temperature. While the low-temperature CCP etching process also failed to realize the anisotropic etching of dislocation sites, the developed PASE-D method demonstrated the ability to effectively reveal the dislocations in SiC wafers regardless of the doping concentration. This will provide designers with a wealth of information for higher quality single crystal SiC wafers in an early stage of the production process in semiconductor manufacturing.

6.3 Elimination of dislocation during molten KOH etching [134]

As revealed in the aforementioned study, PASE-D, which operates at medium temperature, will form etching pits of dislocation, while normal PASE at high temperature will not reveal dislocations. It is rational to propose that the selectivity of dislocation will disappear when the temperature further increases. This mechanism offers an opportunity for chemical etching like molten KOH etching to do fast polishing. In this section, the vanishing process of dislocation etching pits is studied, and the attempt of using molten KOH to do polishing is presented.

6.3.1 Etch pits angle

Molten KOH etching is regarded as the most common dislocation revelation method. Many etch pits of dislocations will form during the etching process, which strongly increases the overall roughness [149]. To obtain a better polishing result, the effect of the etch pits needs to be eliminated. Hartman *et al*. observed that when the temperature increased to >1170°C, a reduction (>95%) of the dislocation density has been observed in silicon because dislocation annihilation is unconstrained by crystallographic glide planes at high temperature [171]. Meanwhile, high-temperature annealing is the most common approach for stress relaxation, which could reduce the level of dislocation [172, 173]. It is reasonable to presume that the revelation of dislocation etch pits is also highly related to temperature.

The relationship between the etch pit angle and the etching time has been first studied. **Figure 6.10(a-e)** shows an in-situ confocal laser scanning microscopy (CLSM) image of an edge dislocation found on the Si face of SiC, and **Figure 6.10(f)** shows their cross-sectional profiles along each solid red line. As the duration time increases, the shape of the etch pits remains the same, but the pits increase in size.

The etch pit angle remains the same. This result suggests that etch pits only get bigger and deeper as the duration increases, while the angle remains unchanged. Thus, to minimize the effect of the etch pits, the etching time should be short.

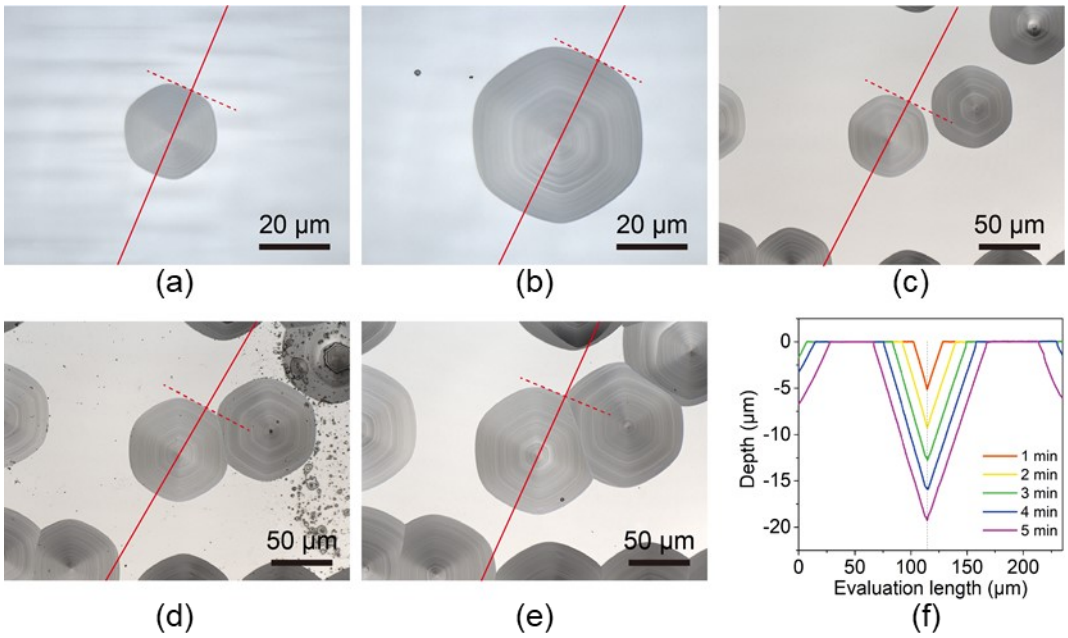


Figure 6.10 In-situ CLSM image of an edge dislocation after etching at 550 °C for: (a) 1 min, (b) 2 min, (c) 3 min, (d) 4 min, (e) 5 min; (f) the cross-sectional profile of (a-e) along the solid red line. The angles are 138.5°, 137.8°, 137.0°, 137.4°, and 138.1°, respectively. [134]

To study the relationship between the etching temperature and the angle of dislocation of the pits, an in-situ study of edge dislocation etching at 500 ℃, 600 ℃, and 700 ℃ for 1 min is shown in **Figure 6.11**. This study shows that with an increase in temperature, the etch pit angle increases. A more systematic diagram of the etching temperature and the etch pit angle is shown in **Figure 6.12**. The etch pit angle of both edge dislocation and screw dislocation, which are the most influential dislocations that increase the surface roughness. Both types of etch pit angles increase with increasing temperature. The speculative mechanism for increasing the etch pit angle with temperature is illustrated in **Figure 6.12(b)**. We assume that the etching rate for the perfect crystal SiC surface is v_0, the etching rate along the horizontal direction is v_H, the dislocation effect-induced increase of the etching rate along the dislocation line is v_D, and half of the etch pit angle is θ. $tan(\theta)$ can be

expressed as **Equation 6.6**:

$$\tan(\theta) = \frac{v_H t}{v_0 t + v_D t} = \frac{v_H}{v_0 + v_D} \qquad v_D > 0 \tag{6.6}$$

as v_D is the increase of etching from dislocation, this parameter should be originated from the localized strain field, which contains elastic energy that reduces the etching energy barrier. v_D should be proportional to the energy associated with dislocation E_D, which is expressed in **Equation 6.7** and **Equation 6.8** [174]:

$$\delta v_D\ (screw) \sim E_D(screw) = \frac{Gb^2}{4\pi} ln\left(\frac{r}{r_0}\right) \tag{6.7}$$

$$v_D\ (edge) \sim E_D(edge) = \frac{Gb^2}{4\pi(1-\nu)} ln\left(\frac{r}{r_0}\right) \tag{6.8}$$

where G is the shear modulus, b is the deformation distance of dislocation, r is the radius from the dislocation centre, r_0 is the radius of the dislocation central core, and ν is Poisson's ratio. From **Equation 6.8** and **Equation 6.9**, it can be found that E_D is proportional to the shear modulus of SiC. According to the mechanical threshold stress (MTS) model, the shear modulus will decrease with increasing temperature [175]. Thus, E_D and v_D will simultaneously decrease with temperature. From **Equation 6.7**, *tan (θ)* was found to increase when v_D decreased. Meanwhile, when v_D becomes 0, the etching shape is represented by the red dotted triangle in **Figure 6.12(b)**. No etch pits remain on the surface. The effect of dislocation is eliminated. It is reasonable to assume that the increase of the etching rate from dislocation will also disappear when the temperature is high enough. Thus, a high temperature is needed to eliminate the effect of etch pits.

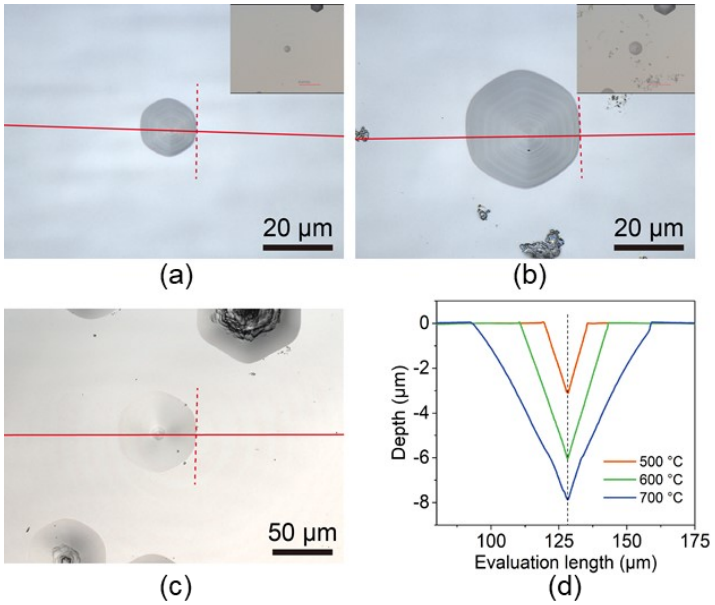


Figure 6.11 In-situ CLSM image of an edge dislocation after etching for 1 min at: (a) 500°C, (b) 600 °C, (c) 700 °C; (d) the cross-sectional profile of (a-c) along the solid red line. The angles are 137.8°, 139.0°, and 153.9°, respectively. [134]

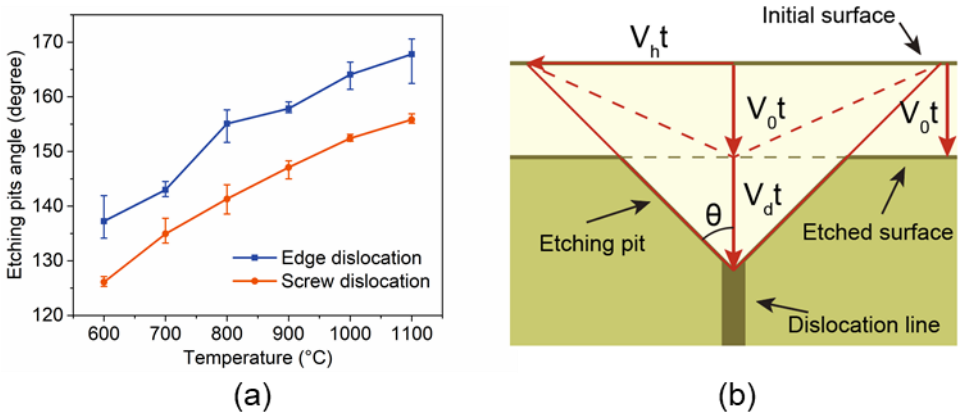


Figure 6.12 (a) The relationship between the etch pit angle and the etching temperature for edge dislocation and screw dislocation after etching at 600 °C - 1100 °C for 2 min, and (b) the schematic of the etch pit formation. [134]

6.3.2 Elimination of dislocation

Based on the assumption in the previous section that high temperature can eliminate the dislocation etching pits, a set of experiments were performed comparing the morphologies of SiC etched at high temperature (1200 °C) and medium temperature (700 °C) for the same duration time (3 min), and the results are shown in **Figure 6.13**. The experiment at 700°C is shown in **Figure 6.13(a)**, where large etch pits of

dislocations can be clearly identified. The dominant dislocation type is edge dislocation. The rest of the perfect crystal surface only shows the intersection of spherical surfaces. The 1200 °C sample is shown in **Figure 6.13(b)** for the same magnification, and the results match our prediction. No large dislocation etch pits were observed, suggesting that the etching enhancement from the dislocation effect had disappeared. Only microscopic hexagonal etch pits were found, which might have been caused during the cooling process, when the temperature goes through a low-temperature range for a short time, inducing low-temperature etchings that could reveal dislocations. This shows that high temperatures can eliminate the effect of dislocations.

However, many circular boss structures were also formed on the high-temperature sample. One of the boss structures is shown in **Figure 6.13(c)**, and the cross-sectional profile along the red dotted line and a 3D image is shown in **Figure 6.13(d)**. This is a typical boss structure with a slashed sidewall. The height of this structure is ~1.64 μm, which strongly influences the surface roughness. The forming mechanism of the boss structure is illustrated in **Figure 6.13(e)**. When the temperature is near the boiling temperature of molten KOH, many vaporized KOH bubbles are generated due to enhanced thermal fluctuation [176]. The bubbles that attach to the SiC surface prevent the spot inside the bubble from contacting in the presence of the surrounding molten KOH. Owing to the significant difference in the reactant flux in the vapour and liquid states, the etching reaction in KOH vapour is much slower than that in molten KOH [177, 178]. The etching speed inside the bubble is lower than that in the surrounding SiC, which is in good contact with molten KOH. Thus, a boss structure is formed on the surface due to the bubble effect.

The results proved that high temperatures could eliminate the selectivity towards dislocation. However, it is currently difficult to use high-temperature molten KOH etching to polish since a high temperature will lead to a bubble effect that increases the surface roughness.

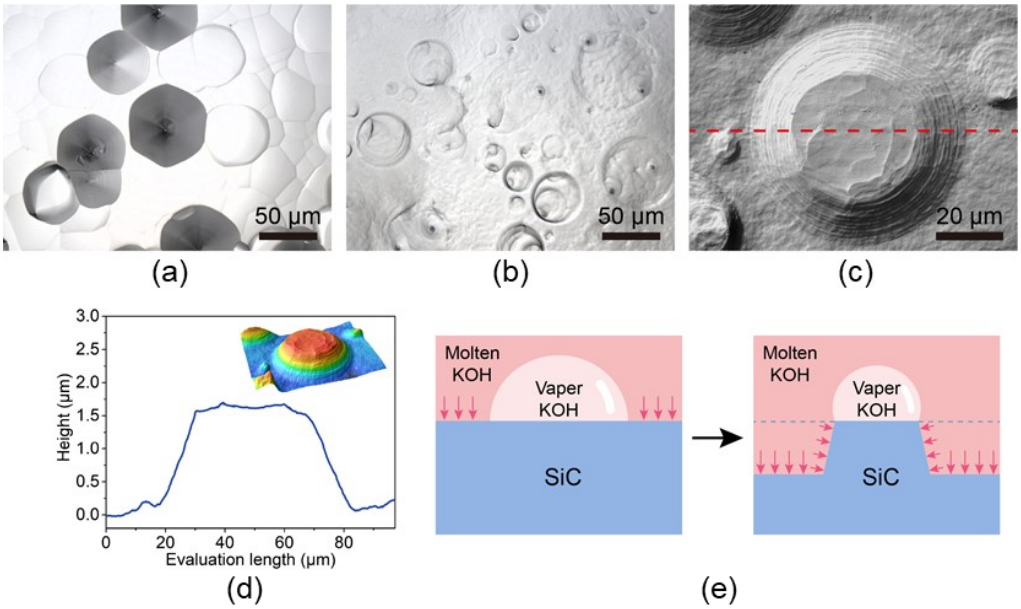


Figure 6.13 CLSM image of the Si face of 4H-SiC after etching at (a) 700 °C for 3 min and (b) 1200 °C for 3 min. (c) Higher magnification of the sample in (b). (d) Cross-sectional profile along the red dotted line in (c). The insert is the 3D image of (c) and (e) the schematic of the boss structure formation. [134]

6.4 conclusion

In this chapter, the selectivity of PASE has been modulated from the atom step-edge to dislocations by changing the temperature. Based on this observation, PASE-D has been proposed and further verified as a promising dislocation detection method. Moreover, the trial of using molten KOH etching to achieve PASE type polishing has been performed.

(1) The conventional molten KOH etching method cannot reveal the dislocations in the highly doped wafer area due to the isotropic electrochemical etching phenomenon. PASE-D is a dry etching process, which can overcome this problem.

(2) PASE-D has demonstrated the ability to effectively reveal the dislocations in SiC wafers regardless of the doping concentration, which can provide designers with a wealth of information to produce higher quality single crystal SiC wafers.

(3) The dislocation revelation process is highly related to temperature. PASE-D

effect can only be achieved at a medium temperature. At a low temperature, the pitting velocity will be small and cannot be observed. At a medium temperature, the velocity difference between pitting of dislocation and etching in a perfect crystal site will be suitable to be observed. At a high temperature, the effect of dislocation is eliminated as the localized strain field is released.

(4) High temperature can also eliminate the selectivity towards dislocation for molten KOH etching. Without preferential etching of dislocation, KOH can be an efficient isotropic etching polishing method for SiC. However, it is currently difficult to use high-temperature molten KOH etching to polish due to the bubble effect near the boiling temperature. It is anticipated that better results can be achieved by inhibiting the bossing effect while increasing the temperature as much as possible.

Chapter 7

Detection and removal of subsurface damage (SSD) [135]

7.1 Introduction

PASE is proved to be a damage-free polishing method with an ultra-fast material removal rate. During the processing of PASE, subsurface damage can be rapidly eliminated. Meanwhile, no new SSD will be introduced into the substrate. It is rational to propose that PASE could be a novel SSD detection method that could facilitate the study of machining of SiC and other difficult-to-machine materials. In this chapter, the feasibility of using PASE for SSD detection has been demonstrated.

4H-SiC has been employed to demonstrate the SSD detection and removal ability of PASE. The 4H-SiC is a typical difficult-to-machine material because of its high hardness and strong chemical inertness[179, 180]. SSDs are more easily introduced in hard and brittle materials during machining. SSD impairs the mechanical, electronic, and optical properties of materials[181-183]. Thus, it is necessary to remove all SSD for advanced applications. As a typical difficult-to-machine material, the processing of SiC wafers usually takes hours, especially the last polishing step, which removes all SSD introduced by the previous slicing, grinding, and lapping steps [184]. The typical MRR of SiC via the CMP method is ~100 nm/h [70]. Moreover, this process consumes a large amount of slurry, which can be toxic, contaminative, and expensive [185, 186]. To minimize the duration of CMP, a precision measurement method of the SSD layer thickness is indispensable.

SSD can be detected using destructive and nondestructive methods. Destructive methods include taper polishing, cross-sectional microscopy, and etching, while non-destructive methods include X-ray scanning, laser scattering, and ultrasonic probing [187]. A non-destructive method can achieve in-process detection and will not destroy the sample. However, the detection accuracy and efficiency are relatively low. Destructive methods, in contrast, are more mature and have better reliability and accuracy. These methods are widely used in industry and academia at present [187]. The most widely used destructive method is taper polishing, which removes the material to form a taper or dimple that crosses the SSD layer to the damage-free matrix and observes the revealed surface to measure the SSD thickness [188]. A material removal method that does not introduce a new SSD is indispensable to operate destructive SSD detection methods. Conventional methods that meet this demand have been applied in SSD detection, including CMP, chemical etching, and MRF [189-191]. For CMP, the main drawback is the low material removal rate for SiC and the massive consumption of slurry, which is expensive and toxic [70, 185, 186]. Chemical etching uses hydrofluoric acid (HF) solution, which is hypertoxic. In addition, SiC does not react with HF at room temperature because of its excellent chemical inertness [115]. Among the destructive methods, MRF is widely used. However, MRF often introduces Fe contamination into the sample [48]. Moreover, the material removal rate is not very high for SiC, and the general MRR is below 0.2 μm/min [42]. To increase the MRR of MRF, diamond abrasives are often used, which might introduce new damage [192]. Furthermore, MRF needs to collocate with a subsequent etching step to open cracks [187]. This etching step will be difficult for SiC because it is inert in all known aqueous etching solutions at room temperature [115]. To further develop the SSD detection technique, a novel SSD-free material removal method is needed.

7.2 Etching characteristics

The PASE-based SSD detection requires polishing of a taper into the substrate. In order to make PASE a predictable tool for taper fabrication, the etching behaviour of PASE has been studied. Here, a 40×40 Si slice was used to explore the profile changes with ICP torch etching. A single spot has been etched on Si for 2 min. Optical photos of the samples are shown in **Figure 7.1(a),** where 1 is the as-received sample, and 2 is the sample after single spot etching by PASE. The size of the pits is approximately 3 cm. Since the ICP torch used in this study has a diameter below 2 cm, the larger etching pits are due to the deflection of the plasma jet when it hits the sample surface and the flow and diffusion of radical. The cross-sectional profile of 1 and 2 along the diagonal is shown in **Figure 7.1(b)**. The profile change exceeds the size of the etching pits and stretches to the entire surface. Because of reaction consumption, a limited lifetime, and dilution by air, the concentration of etching radicals decreases as the distance from the torch increases. Thus, the etching depth decreases along the pit radius.

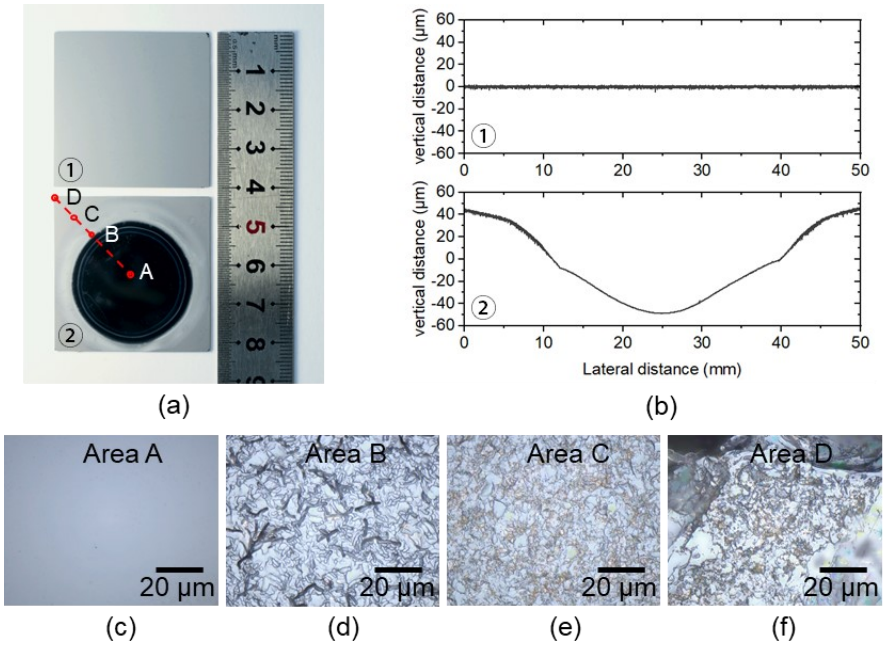


Figure 7.1 (a) Optical photo of the ICP etching samples: 1. As-received sample, 2. etched sample; (b) the cross-section profile alone the diagonal of samples 1 and 2, respectively; (c)-(f) the CLSM image of area A-D in Figure 4(a), respectively. [135]

More detailed high magnification photos are shown in **Figures 7.1(c)-(f)**. **Figures 7.1(c)** and **7.1(d)** show areas A and B of the etched sample, where A is the centre of the etching pit and B is the edge of the etching pit. The initial rough and the damaged surface cannot be observed in the CLSM image of area A, implying a thorough etching of the SSD layer. The opening of cracks can be observed in area B, suggesting that less complete etching occurred at the edge of the pit due to the lower concentration of etching radicals. **Figures 7.1(e)-(f)** shows the area outside the etching pit. The yellow and grey particles on the surface area should be the deposited fluorocarbon polymers [193]. This result could explain the profile change outside the etching pits, where accumulated fluorocarbon polymer covers the initial surface. Furthermore, the adsorption of deposited particles increases with decreasing temperature, which is consistent with the distance from the heat source, i.e., the plasma centre. Consequently, the entire initial surface of the sample will be deformed, either by etching from plasma or occlusion by deposition particles, and it is impracticable to identify the raw surface after unobstructed etching. Nevertheless, marking the position of the raw surface is crucial in destructive SSD detection; hence, a raw surface protective countermeasure is needed during ICP etching [187].

7.3 SSD detection

Masks of photoresist or deposited metal are often used in the plasma etching process to protect certain areas. In this study, a mask has been used for that purpose. To resist the high temperature and highly reactive radicals from the ICP torch, a slice of 4H-SiC has been used as the mask.

The entire rapid SSD measurement process can be described as follows: 1. ICP is ignited as described in the experimental setup section. 2. As illustrated in **Figure 7.2**, the SiC sample for the SSD measurement is partially covered by a smaller piece of SiC to protect a portion of the original surface as a reference plane to measure the SSD depth. 3. The covered sample is then moved directly under the ICP flame

by the 3-axis NC platform and etched for 2 min. 4. After etching, the SiC cover is released, and the etched SiC sample is cleaned with DI water and alcohol. 5. After cleaning, the etching profile is observed via CLSM. The depth of the SSD layer is obtained by comparing the vertical distance between the original protected surface (z_1) and the last trace of the SSD layer (z_2).

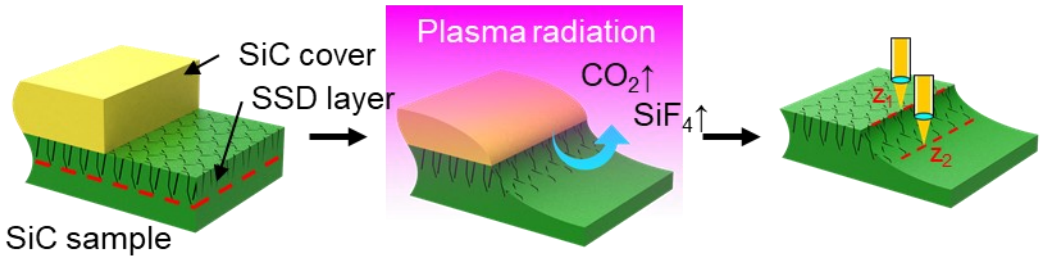


Figure 7.2 The schematic diagram of the SSD detection process. [135]

A taper that gradually deepens is needed to observe the SSD depth successfully. Considering the ease of CLSM operation and avoiding stitching measurement to ensure accuracy, the lateral length of the taper should be controlled within 100 μm. Moreover, the etching rate should increase along the exposed sample surface and cover the 100 μm observation zone mentioned above. The etching rate is governed by the Arrhenius equation listed in **Equation 5.3**. Thus, only the temperature and radical concentration are needed to study. According to **Figure 7.1**, the lateral distance between the plasma centre and the sample ($d_{p\text{-}s}$) significantly affects the etching behaviour. Hence, the influence of $d_{p\text{-}s}$ on these two factors that affect the etching rate was studied using COMSOL Multiphysics.

Figures 7.3(a)-(c) show the temperature simulation of the etching process for three sample positions in which dp-s equals 0.5 mm, 5 mm, and 9 mm. **Figure 7.3(d)** shows the temperature of the observation zone, which is on the surface of the sample and ranges from the mask boundary to the exposed part of the sample 100 μm away horizontally. With increasing dp-s, the sample moves to the edge of the plasma, and the temperature gradually decreases. However, the temperature of each sample is uniform, fluctuating within 1 °C. This result might be due to the excellent

thermal conductivity of SiC. Thus, the etching rate difference due to temperature change can be neglected. As the calculation of the reactive radical concentration on the surface can be complicated, the plasma flow rate was studied as an approximation to facilitate the investigation. **Figures 7.3(e)-(g)** show the simulation of the flow rate of the three experiments. The flow rate on the sample surface should be zero. Here, the flow rate was collected from the area 10 μm above the observation zone, the aforementioned indicator of the flow condition near the surface, and the data are plotted in **Figure 7.3(h)**. The velocity variation increases with dp-s. A larger flow rate change induces a larger etching rate difference. Accordingly, the sample stack should be placed in the outer region of the plasma, and dp-s = 9 mm has been used in the subsequent experiments.

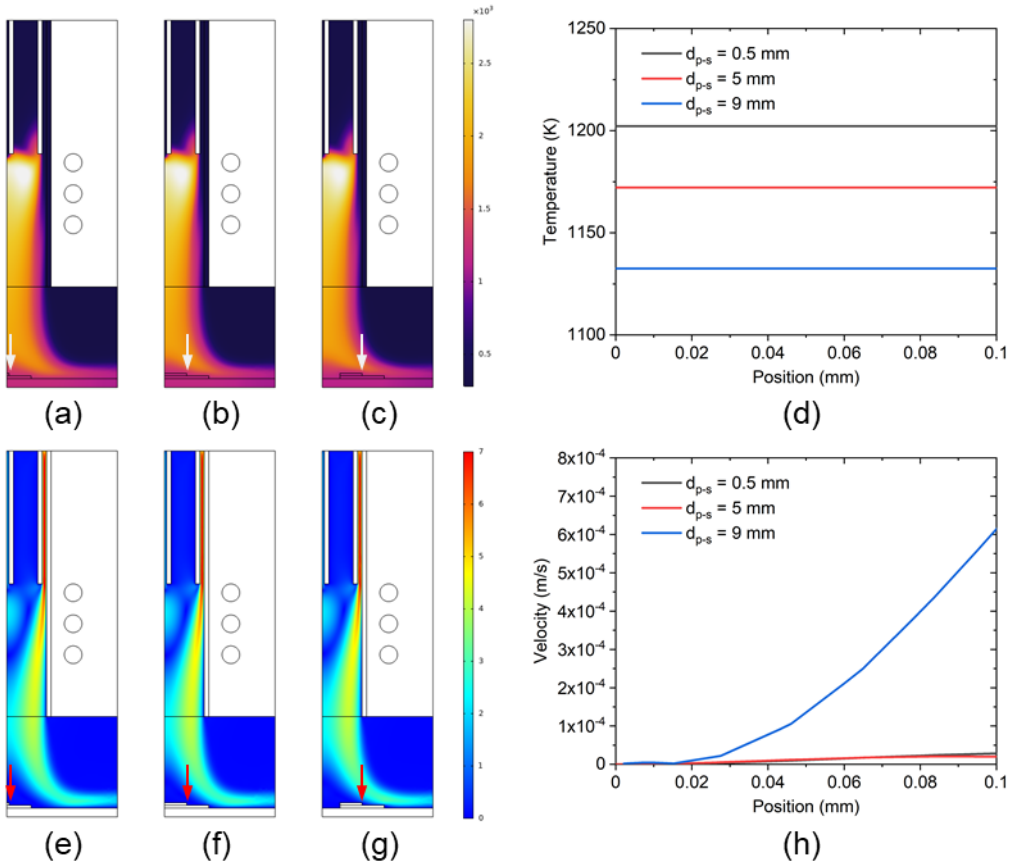


Figure 7.3 (a)-(d) Temperature simulation of the ICP torch, the colour legend of (a)-(c) is shown to the right of (c); (e)-(h) flow velocity simulation the ICP torch, the colour legend of (e)-(g) is shown to the right of (g). [135]

PASE for SSD measurement was conducted on the Si face of the SiC sample with a SiC cover and d_{p-s} = 9 mm. The morphology changes before and after etching are shown in **Figure 7.4**. The lapped SiC surface (**Figure 7.4(a)**) shows an actinomorphic trajectory pattern, which is caused by the periodic eccentricity lapping process [194]. **Figure 7.4(b)** shows the same sample after etching reveals SSD. The left part is the covered area, where no visual difference can be observed. The right part is the etched area, where a glazed surface implies the removal of the damaged layer. A distinct boundary is observed between the covered and etched areas. **Figure 7.4(c)** is a schematic of the etching boundary area, which is marked by the red rectangle in **Figure 7.4(b)**. The red arrows 1-3 represent the covered area, transition etched area, and completely etched area, which are shown in **Figures 7.4(e)-(g)**, respectively. **Figure 7.4(d)** is the SEM image of the original surface. No discrepancy can be observed within the area of the etched SiC sample under the protection of the SiC cover (**Figure 7.4(e)**), which indicates that the SiC cover efficiently suppresses the etching of SiC beneath it. Thus, the surface under the SiC cover can be used as a reliable initial reference plane for measuring the thickness of the SSD layer. **Figure 7.4(f)** shows the area near the edge of the SiC cover, where the radical flow can reach and react with the sliced SiC sample surface. Meanwhile, the edge of the SiC cover confines the radical flow from some directions; thus, the SSD layer is only partially removed. Many cracks are revealed by the plasma etching, suggesting that the revealed plane is inside the SSD layer. **Figure 7.4(g)** shows the surface of the sliced SiC sample far from the protection of the SiC cover. Without any protection, the SSD layer is fully etched. Cracks completely vanish on the surface, indicating a damage-free surface [187]. The protrusions remaining on the surface are caused by the uneven etching rate between the damaged layer and the damage-free matrix [195]. ICP etching in this part crossed the bottom of the SSD layer.

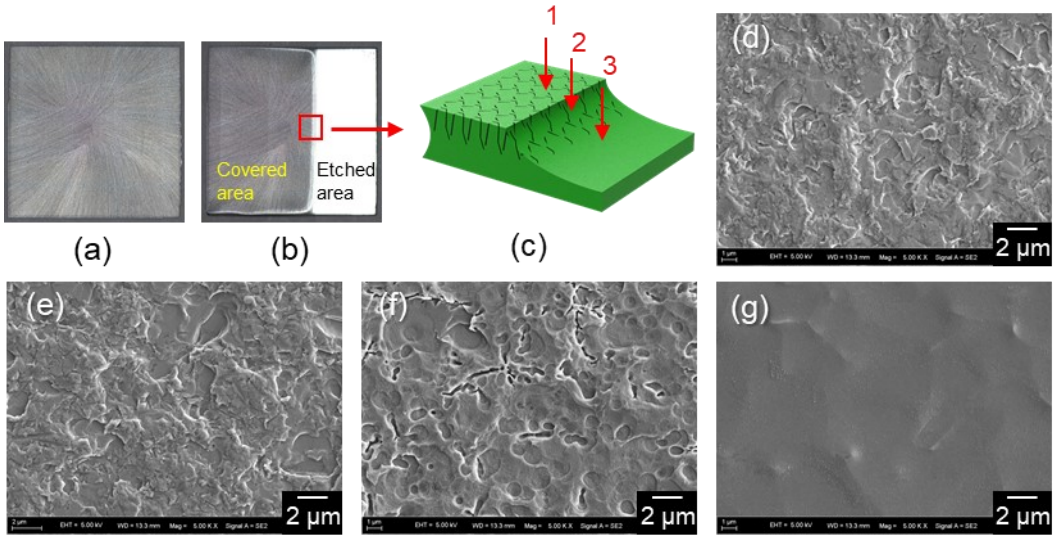


Figure 7.4 The optical photo of the (a) as received lapping SiC and (b) etched SiC; (c) the schematic diagram of the etching boundary in (b); SEM micrograph of (d) as received sliced SiC surface; (e) area 1 under the protection of SiC cover after etching; (f) area 2 near the boundary of SiC cover and (g) area 3 without the protection of SiC cover. [135]

To measure the vertical distance between the original surface and the bottom of the SSD layer, CLSM has been employed, and the results are shown in **Figure 7.5**. The 2D CLSM image is shown in **Figure 7.5(a)**, and the 3D image is shown in **Figure 7.5(c)**. A very clean taper was formed via ICP etching. For **Figure 7.5(a)** and **Figure 7.5(b)**, the left side of the SiC sample was exploded under ICP, while the SiC cover protected the right side. The right side retained its original morphology, suggesting that no etching occurred in this area, which agrees with the SEM result in **Figure 7.4(e)**. The left side underwent etching of dense ICP, and the original morphology was totally removed. A slope structure caused by the partial protection of the SiC cover edge links the original surface and deeply etched area. A gradual reduction in crack density can be observed along the taper, analogous to that of the MRF taper method, representing thinning of the SSD layer [196]. The deepest crack disappears in the bottom of the SSD layer. After that spot, all SSDs were removed, and only perfect SiC remained. A cross-sectional profile was extracted along the last crack trace, as depicted in **Figure 7.5(b)**. The red rectangle in **Figure 7.5(b)** indicates the position of the last crack. The vertical distance to the original surface is 1.128 μm, which is also the depth of the SSD layer. **Figure 7.5(b)**

also demonstrates that the total etching depth is approximately 4 μm, which is more than three times the measured SSD layer thickness. In this case, the etching depth is sufficient to penetrate the SSD layer, suggesting that the result is accurate.

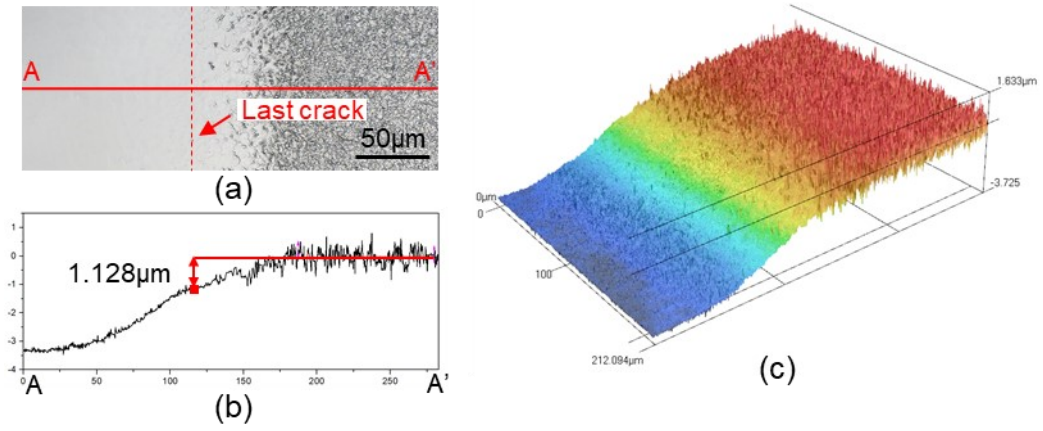


Figure 7.5 (a) the CLSM image of the etched slope of the sliced SiC sample; (b) the cross-sectional profile along A-A'; (c) the 3D image of (a). [135]

To further confirm the accuracy of the SSD measurement, FIB was used to cut a cross-section of the etched sample, and STEM was employed to observe the SSD layer directly. **Figure 7.6(a)** shows the area under the protection of the SiC cover: cracks, stress, and amorphous layers can be clearly observed. The depth of the SSD layer is approximately 1.06 μm, which matches the ICP etching sample. Higher magnification images of areas A and B are shown in **Figures 7.6(b)-(c)**, which represent the typical crack region and deformed region of the SSD layer. The cross-section of the part where SSDs are thoroughly removed by ICP etching is depicted in **Figure 7.6(d)**. A visually uniform SiC interface was observed, indicating that the SSD layer had been removed. The HRTEM of the interface region shown in **Figure 7.6(e)** further proves this point. Perfectly crystalline 4H-SiC has been observed immediately below the interface, and the image corresponds to the <11-20> face of 4H-SiC [197]. This result proves that only a single crystal 4H-SiC remained on the crack-free surface formed by ICP etching, and no new SSD was introduced. The selected area electron diffraction (SAED) pattern in **Figure 7.6(f)** shows a typical diffraction pattern along the [11-20] zone axis of 4H-SiC, which agrees with the

HRTEM image and further supports the excellent crystallinity of the remaining substrate [198]. The results demonstrate that ICP etching of SiC is a rapid, SSD-free method that produces accurate SSD measurements, making it a promising approach for SSD detection of SiC.

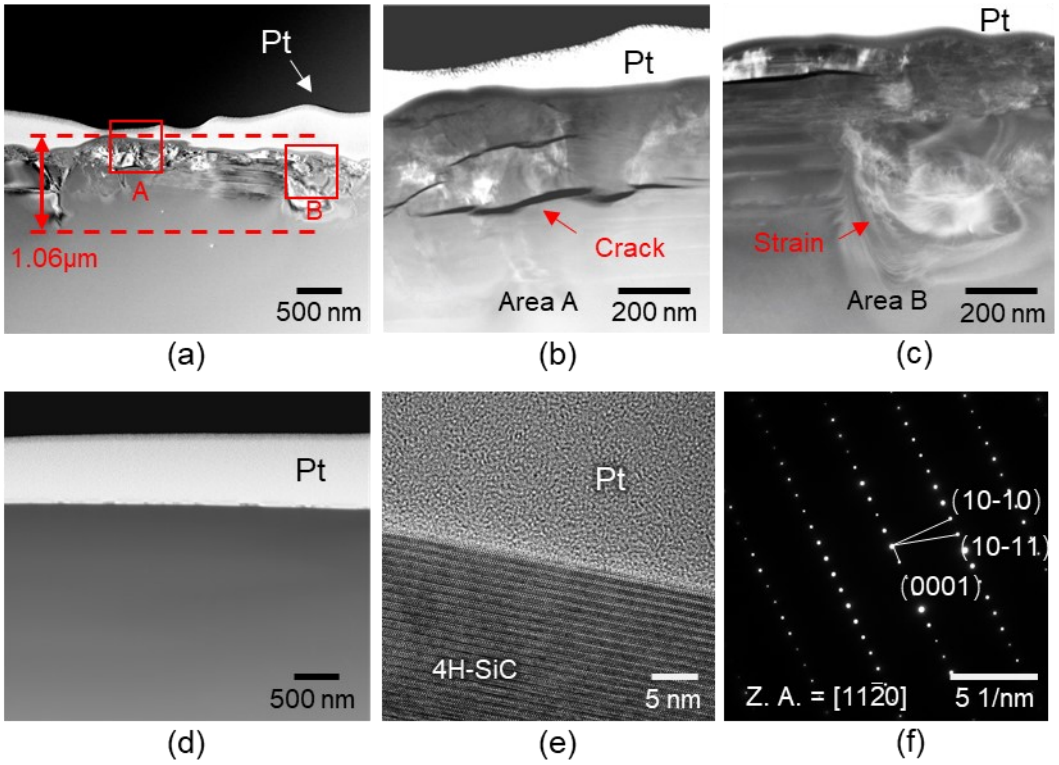


Figure 7.6 Subsurface investigation performed by STEM: (a–c) STEM images of the as-ground SiC surface, obtained with different magnifications; (d) STEM image of the ICP etched SiC surface; (e) HRTEM image of the ICP etched SiC surface; (f) selected area electron diffraction pattern of the ICP etched SiC surface. [135]

7.4 Rapid SSD screening demonstration

The ability of the PASE method to rapidly and accurately detect the thickness of the SSD layer enables us to quickly screen and find the optimal lapping parameters. This rapid screening ability has been demonstrated here, using PASE to study the influence of lapping parameters, including granularity, lapping pressure, and revolution velocity. Twelve sets of samples were lapped using the parameters listed in **Table 8**.

With the assistance of rapid PASE, only 2 min of etching is needed to reveal the SSD layer of each sample. The system operates in an atmospheric environment, which eliminates the time-consuming vacuum process in typical plasma etching. In addition, this method does not require a subsequent etching step for opening cracks, which is indispensable for the traditional MRF method. Furthermore, the NC platform can load multiple samples. The entire SSD revelation process for 12 samples is completed within 30 min.

Table 8 Lapping parameters for SSD detection [135]

#	Pressure (kPa)	Granularity (mesh #)	Revolution velocity (rpm)
1	50	1000	150
2	100	1000	150
3	150	1000	150
4	200	1000	150
5	50	500	150
6	50	1000	150
7	50	2000	150
8	50	3000	150
9	50	1000	50
10	50	1000	100
11	50	1000	150
12	50	1000	200

Figure 7.7(a) shows the influence of lapping pressure on the MRR and SSD of the SiC sample (sample number 1-4). MRR increases linearly with increasing pressure. However, the SSD changes at a much lower rate because the gap between the sample and diamond disc decreases with increasing lapping pressure. The number of abrasive particles that undertake the load increases, so the contact pressure remains constant. This causes the relevant SSD thickness to remain

constant [199]. However, the MRR increases quickly as the number of effective abrasive particles increases. Granularity has a similar influence over the MRR and SSD layers (sample number 5-8), as shown in **Figure 7.7(b)**. This is because grain size directly affects the cut depth of each grain. In **Figure 7.7(c)**, representing sample numbers 9-12, the MRR increases with the revolution velocity because a higher cutting speed removes more material in unit time. However, if cut depth remains the same, no obvious changing trend of SSD can be observed, which means that SSD is not sensitive to lapping revolution velocity. In summary, granularity has the most significant effect on SSD thickness, followed by pressure. Revolution velocity has no apparent influence on SSD thickness.

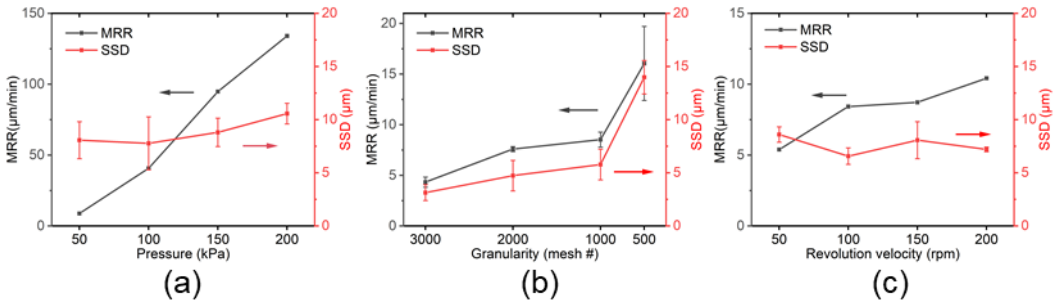


Figure 7.7 Influence of (a) pressure (sample number 1-4), (b) granularity (sample number 5-8), and (c) revolution velocity (sample number 9-12) on SSD and MRR of SiC. [135]

7.5 Conclusion

In this chapter, PASE, an SSD-free material removal method, has been used to perform rapid SSD detection of SiC. Results indicate that PASE is a promising SSD detection method. It is rational to further propose that by altering the composition of the etching gas, PASE could be a general method for SSD detection of a wide range of materials.

(1) The plasma diagnosis and etching behaviour study have shown that PASE has the capability of fast material removal. The lateral distance between the plasma centre and the sample (dp-s) significantly affects the etching behaviour.

(2) The temperature simulation shows the difference is independent of the increase of dp-s due to the excellent thermal conductivity of SiC. The plasma flow simulation has been performed to optimize the etching position. Also, a SiC mask has been utilized to protect the reference surface, and rapid SSD detection has been completed within 2 min.

(3) As confirmed by STEM, the PASE process has not introduced a new SSD, and the SSD layer thickness determined by STEM has matched well with that of the PASE method.

(4) A demonstration of rapid scanning has been performed on 12 samples to analyze the influence of lapping parameters on SSD. It is suggested that PASE could be a very promising rapid SSD detection method.

Chapter 8

Summary and prospect

8.1 Summary

In this thesis, a novel polishing method called plasma-based atom selective etching (PASE) is proposed. PASE is a non-contact polishing method that can achieve damage-free and atomic precision polishing with an ultra-high MRR. Apparatuses based on CCP and ICP have been developed and optimized to implement PASE. The mechanism has been speculated from the observation of results and further verified by both experiments and simulations. A broad range of third-generation semiconductor materials, including SiC, GaN, AlN and Al_2O_3, have been polished by the proposed PASE to demonstrate its versatility.

In **Chapter 1**, two motivations of this work have been presented: 1. Addressing the problem of polishing 4H-SiC and other difficult-to-machine third-generation semiconductor material; 2. Developing a state-of-the-art polishing technique to approach the polishing limits and achieve the truly-atomically flat surface. Furthermore, the structure of the thesis has been briefly provided.

In **Chapter 2**, the state-of-the-art methods have been reviewed for solutions to the efficient polishing of 4H-SiC, and a potential approach to truly-atomically flat surfaces has been provided. Following that, PASE has been proposed.

(1) The background of WBG material, especially 4H-SiC, has been introduced. The whole wafer manufacturing process has been introduced to clarify the status of

ultra-precision polishing of semiconductors, which is the main focus of this research.

(2) The state-of-the-art ultra-precision methods have been reviewed, the available techniques for the fabrication of near-perfect surfaces have been presented. The merits and demerits of those methods have been summarized. Furthermore, the conclusion is that a highly reactive method is demanded for high MRR.

(3) To achieve highly reactive etching, AP-plasma has been introduced. The current AP-plasma-based method, including PCVM, PJM, RAPT, APPP, and AEPM, has been presented. AP-plasma, especially ICP based plasma etching, has the capability to achieve high MRR. However, the surface roughness often deteriorates after etching.

(4) Based on AP-plasma, the PASE method has been proposed. PASE retains the advantage of high MRR by AP-plasma etching. Unlike other AP-plasma-based methods, which have relatively low precision due to isotropic etching, the polishing mechanism of PASE is based on selective removal of atoms that form roughness and has a precision toward an atom level. It can be a potential solution to fabricating a large-area near-perfect surface. Meanwhile, PASE is a universal technique that could be applied to various single-crystal materials.

In **Chapter 3**, the background of three groups of etching apparatus, including CCP etching, ICP etching, and KOH etching, have been introduced, and their optimization processes have been investigated for practical applications.

(1) The CCP device has been developed for low-temperature etching. The configuration, electrode material, and cooling system have been studied for the optimal device, which has utilized the remote type nozzle with aluminon electrode material and a water-cooling system.

(2) The ICP etching device has been developed for high-temperature etching. A detachable ICP torch has been built to reduce the cost. Then, different sample

holders have been made to control the sample temperature. Also, several environmental control strategies have been developed to prevent contamination from the ambient atmosphere.

(3) The crucible-less ultra-high temperature KOH etching device has been developed to further test the etching properties under a wide range of temperatures. The experimental setup has offered a fast approach to etching at 1200 °C without pollution from the crucible.

In **Chapter 4**, the demonstration of PASE has been conducted based on ICP etching with a heat-insulated sample holder made of alumina foam. Results show that PASE can produce a large-scale truly-atomically flat surface with an ultrafast speed. This method can be a potential solution to the problem of mass-producing atomically flat surfaces of single-crystal materials and foster the applications of third-generation semiconductor materials and the innovation of advanced technologies.

(1) Plasma diagnostics show that the ICP jet contains abundant F and O radicals capable of conducting the etching of SiC. Meanwhile, ICP serves as a heat source that can heat the sample over 1400 °C in 60 seconds.

(2) Typical flat-bottom morphology can be observed during PASE, confirming the lateral etching effect. The AFM and TEM results show that PASE can achieve a truly-atomically flat surface. Meanwhile, it is noted that the speed of this method is more than 1000 times faster than conventional polishing method and can be used for high throughput production.

(3) The universality of PASE has been demonstrated by etching various single-crystal materials that resulted in an atomic roughness and an ultrahigh speed.

In **Chapter 5**, the mechanism of PASE etching 4H-SiC has been discussed. The optimized experiment condition for PASE has been identified. The related mechanism speculation to achieve PASE has been discussed, and AIMD simulations have helped to prove the mechanism.

(1) In the preliminary experimental study, the PASE condition has been achieved under a certain stand-off distance. The influencing conditions were then decoupled into temperature, reactant composition, and flow rate for discussions.

(2) The subsequent experiment suggests that the low-temperature etching results in pitting and PASE can be realized only at high temperatures. When the temperature is above 1300 ℃, PASE can be achieved but remains insensitive to the further rise in temperature. The optimum reactant composition ratio (CF_4:O_2) for PASE is in the range of 12:11 to 4:3. A higher or lower composition ratio will lead to carbon/fluorocarbon film deposition or SiO_2 accumulation, respectively.

(3) In addition, the surface free energy minimization causes spontaneous faceting for the vicinal angle sample and helps polish the on-axis 4H-SiC samples. The high-index facet that forms the surface roughness will be removed due to higher surface free energy than the basal plane (0001).

(4) Simulation results show that F indicates selectivity towards step-edge during the etching process at all temperatures. However, the selectivity of F etching decreases with increasing temperature.

(5) The etching of SiC using F causes amorphous carbon accumulation. that hinders the step-edge and vanishes the selectivity; ultimately, F cannot remove the carbon layer. It matches well with the experimental results observed when the oxygen concentration is low.

(6) The introduction of oxygen can remove the carbon layer, and the removal ability increases significantly as the temperature increases. Meanwhile, oxygen shows selectivity towards step-edge at high temperatures and can produce a loose Si-O structure, facilitating the etching and further increasing the overall selectivity for the F/O mixture plasma towards step-edge.

(7) For F/O mixture plasma, oxygen is the key element that needs high temperature

to promote selectively etching. High temperature can increase the removal rate of amorphous carbon by oxygen and increase the selectivity towards step-edge for oxygen. At high temperatures, F and O can selectively etch Si and C, respectively. The synergy of F and O is the key to achieving a highly efficient etching of step-edge of SiC. Hence, high temperature and appropriate F/O ratio are two indispensable conditions to achieve PASE.

In **Chapter 6**, the selectivity of PASE has been modulated from the atom step-edge to dislocations by changing the temperature. Based on this observation, PASE-D has been proposed and further verified as a promising dislocation detection method. Moreover, the trial of using molten KOH etching to achieve PASE type polishing has been performed.

(1) The conventional molten KOH etching cannot reveal dislocations in the highly doped wafer area due to the isotropic electrochemical etching phenomenon. PASE-D is a dry etching process, which can overcome this problem.

(2) PASE-D has demonstrated the ability to effectively reveal dislocations in SiC wafers regardless of the doping concentration, which can provide designers with a wealth of information to produce high quality single-crystal SiC wafers.

(3) The dislocation revelation process is strongly related to temperature. PASE-D effect can only be achieved at a medium temperature. At a low temperature, the pitting velocity will be small and cannot be observed. At a medium temperature, the velocity difference between pitting of dislocation and etching in a perfect crystal site will be suitable to be observed. At a high temperature, the effect of dislocation is eliminated as the localized strain field is released.

(4) High temperature can also eliminate the selectivity towards dislocation for molten KOH etching. Without preferential etching of dislocation, KOH can be an efficient isotropic etching polishing method for SiC. However, it is currently difficult to use high-temperature molten KOH etching to polish due to the

bubble effect near the boiling temperature. It is anticipated that better results can be achieved by inhibiting the bossing effect while increasing the temperature as much as possible.

In **Chapter 7**, PASE, an SSD-free material removal method, has been used to perform rapid SSD detection of SiC. Results indicate that PASE is a promising SSD detection method. It is rational to further propose that by altering the composition of the etching gas, PASE could be a general method for SSD detection of a wide range of materials.

(1) The plasma diagnosis and etching behaviour study have shown that PASE has the capability for fast material removal. The lateral distance between the plasma centre and the sample (dp-s) significantly affects the etching behaviour.

(2) The temperature simulation shows the difference is independent of the increase of dp-s due to the excellent thermal conductivity of SiC. The plasma flow simulation has been performed to optimize the etching position. Also, a SiC mask has been utilized to protect the reference surface, and rapid SSD detection has been completed within 2 min.

(3) As confirmed by STEM, the PASE process has not introduced a new SSD, and the SSD layer thickness determined by STEM has matched well with that of the PASE method.

(4) A demonstration of rapid scanning has been performed on 12 samples to analyze the influence of lapping parameters on SSD. It is suggested that PASE could be a very promising and rapid SSD detection method.

To sum up, the major contributions to knowledge by this work are:

(1) A novel ultraprecision polishing method, called PASE, has been proposed for the first time. It has been demonstrated that PASE has the capability to reach atomic level roughness with an ultrafast MRR of more than 1000 times of the

conventional CMP method. Meanwhile, the universality of PASE has been verified on various difficult-to-machine crystal materials. The PASE method can reduce the cost and accelerate the serial production of WBG wafers.

(2) Atomically flat surface with PASE, which is the roughness limit and the reflection of precision limitation for manufacturing a flat surface, could be achieved. Theoretically, PASE can achieve a truly-atomically flat surface due to atomic level selectivity. The HRTEM and AFM results suggest that such a limit could be achieved, but more evidence is required. PASE provides a possible solution to fabricating large-scale truly-atomically flat surfaces, facilitating many advanced applications, including quantum computing.

(3) A speculation of the mechanism of PASE has been provided based on simulations and experiments. The PASE of SiC is caused by atom step-edge selective etching originated from a synergy effect of CF_4 and O_2 plasma, which is highly related to temperature. Meanwhile, the surface free energy minimization effect also facilitates the polishing process.

(4) The dislocation revelation and elimination process during PASE have been discussed. Based on these results, a novel dislocation detection method called PASE-D has been proposed. It is observed that the etching selectivity can be switched from atom step-edge in PASE to dislocation in PASE-D by temperature modulation. Results have provided an insight into a possible means to achieve PASE with wet etching or chemical etching, which could significantly reduce the cost and increase the applicability of PASE.

(5) Based on the properties of fast damage-free etching, PASE has been applied for SSD detection. The mask used in the SSD detection for taper fabrication has provided a choice of the processing strategy of PASE.

8.2 Recommendations for future work

PASE has been demonstrated to have an ultrahigh MRR and atomic level roughness in a local area throughout the studies in this thesis. In particular, it has been noted that an extremely low roughness of 0.05 nm on SiC can be obtained about 1000 times faster than the existing state-of-the-art method (e.g., modified CMP). PASE has also been tested on various materials, including SiC, Al_2O_3, GaN, Si, and AlN, for its universality. Then, the speculation of the selective mechanism has been discussed. Moreover, more applications, e.g., dislocation detection and SSD detection, have proved the advances of PASE. This work opens a new field of research. There are a few key problems that would be very valuable for future work:

1. Large-scale PASE. PASE has been demonstrated only for small samples (10×10 mm^2). Although we have tried using PASE as a sub-aperture method and a scan path to polish large-scale wafers, the results are not ideal due to uneven etching and thermal effects. Based on the mechanism of PASE, it could be ideal for producing a large-scale PASE environment to process the whole wafer at one time. Creating a reactional environment with uniform temperature and reactive species could be critical.

2. Decouple the etching parameters of PASE. In this thesis, the etching parameters have not been perfectly decoupled. For instance, since plasma is also the heat source in this study, increased plasma intensity will always lead to a rise in temperature. Besides, the cone shape of the plasma jet will result in a change of beam size with the increase of stand-off distance, resulting in a difference in the utilization rate of the plasma. The oxygen from the ambient environment will also affect the accuracy of the experiment. To accurately study the influence of the PASE parameters, an environment control PASE with an ultrahigh temperature heating platform will be very useful. Finding the optimized stand-off distance in environment control circumstances (for instance, in a vacuum chamber) can eliminate the influence of ambient oxygen and thus maximize the utilization rate of the plasma jet.

3. Dislocation elimination. One remarkable difference between PASE and other

chemical etching is that PASE will not preferentially attack the dislocation site. The mechanism has been briefly described in this thesis that high temperature will release the stress of dislocation site and thus the selectivity will disappear. However, this conclusion needs direct evidence. Since this process is significant as it determines the polishing effect, it requires a more extensive research focus.4. Thermal stress. PASE is an etching process with local high temperatures, and it is inevitable to introduce thermal stress into the sample, which could change the material performance and reduce the fatigue life. In this thesis, the phenomenon is not very prominent since the SiC has high thermal conductivity and the sample is small. It is important to investigate the influence of thermal stress introduced by PASE. Also, the stress elimination method like thermal annealing should be considered.

5. Quantitative study on the morphology evolution using numerical simulations, for instance, atomistic kinetic Monte Carlo (KMC) simulations. The KMC simulations can be used to understand the PASE process better. Furthermore, using the simulation module, the polishing results could be predicted based on the inputs of experimental parameters. The simulation could also help in finding the suitable materials that PASE can adopt for rapid polishing.

6. Applicability of other crystal materials. As the PASE with SiC, Al_2O_3, GaN, Si, and AlN have been briefly tested in this thesis, the universality of PASE has been verified. PASE is a promising method for polishing more materials. Single crystals with high molting temperature and layer-by-layer structures are preferable. The mechanism of realizing PASE for each material might be different, requiring more research accordingly.

7. Using chemical etching to realize the PASE effect. The mechanism of PASE is selectively etching of atoms of a specific position and does not necessarily require the use of plasma. If the selective etching can be amplified, using any highly reactive chemical could be possible. In this thesis, molten KOH has been an attempt

to replace ICP. However, the result shows that the PASE condition for KOH is a high temperature, which is higher than its boiling point. It is suggested that KOH etching at high pressure, which could increase its boiling point, could be a better strategy. Meanwhile, using gas-phase chemicals (*e.g.,* F_2, ClF_3) for etching at high temperatures could also be considered. If the chemical-based PASE can be realized, the problem of developing a large-scale plasma device can be bypassed and thus can facilitate the realization of large-scale PASE.

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