Assessment of the Switching Characteristics of a commercial e-mode Power GaN Device Using a Dual Pulse Test Set-up

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***Abstract*—Power density and efficiency are amongst the design features that are becoming extremely important in today's power electronics systems. Power switches made from Gallium Nitride (GaN) materials have recently become available commercially, allowing switching operations at considerably higher frequencies and hence making efficient and compact design possible for power converters. However, because of the unique structure of the power GaN switches which differ from conventional Si-based transistors, it is essential to realise their dynamic performance characteristics. In this paper, the dynamic response of an e-mode power GaN switching device made from Infineon (IGO60R070D1 650V/31A) is analysed using a dual pulse test (DPT) experiment. The switching characteristics of the device are investigated showing that special considerations are required to achieve reliable performance. In addition, a switching loss model is proposed based on the DPT results for the determination of both turn-off and turn-on switching losses at various operating conditions. The loss model can subsequently be used for design optimisation of the GaN power converters and their cooling systems for various applications such as automotive and photovoltaic systems.**

Keywords—device under test, dual pulse test, dynamic response, power GaN devices, rise time and fall time, switching losses.

I. INTRODUCTION

In modern power electronics system design and operation, it is important to achieve high efficiency and power density, specially for the applications such as automotive and electric vehicles, where system size, volume and energy efficiency are among the key system requirements. Semiconductor devices are at the heart of power converters and they are key in achieving higher efficiency and power density. Passive components such as inductors, usually occupy most of the converter space. Although the size of passive components can be significantly reduced by increasing the operating frequency, this is challenging for Silicon (Si) based devices due to the inherent limitations in their material properties [1]–[3].

High electron mobility transistors (HEMTs) such as Gallium Nitride (GaN) devices show promising performance as they can operate at substantially higher frequencies and maintaining the efficiency at acceptable level. There is a 2-Dimensional Electron Gas (2DEG) channel in the structure of GaN switches resulted from the crystal polarity between GaN and AlGaN buffer layers. The 2DEG channel provides an adequate path for conduction between the source and drain of the device [2], [4]. Therefore, GaN switches have the capability of switching at high frequencies up to 1MHz [5]. In comparison to Si-based switches, GaN devices have a lower gate voltage threshold, lower gate breakdown voltage, lower on-resistance, and smaller device capacitance [4], [6], [7]. Nevertheless, their unique structure and characteristics require specific considerations for their practical implementation.

GaN switches are mostly available in lateral structure and they are produced in two types, i.e. depletion mode (d-mode) and enhancement-mode (e-mode). The d-mode devices normally operate at on state that can be turned off by applying a negative voltage across their gate and source terminals. This is in contrast to the e-mode GaN switches, which normally operate at off state similar to the conventional transistors. Detailed information about the structure of the GaN devices can be found in [4]. Recently, power GaN transistors have become commercially available and Table I compares the key parameters of currently available GaN switches in the market.

Because of the superior characteristics of GaN devices, they can be used effectively in hard-switching applications where, the switching losses have the largest contribution to the total power losses. There are only few papers that study the dynamic performance of GaN devices and their associated losses. Huang et al. [1] present an experimentally verified loss model for d-mode power GaN devices taking into account the parasitic elements and nonlinearity of the capacitors and transconductances. Ji et.al. in [8] analysed the dynamic response of a d-mode vertical GaN transistor. The presented model was simulated by utilising ATLAS and SPICE software. In this model, the parasitic capacitors were distributed inside the device package. It has been concluded that the simulated model can be used for comparing the performance of the GaN devices with the conventional semiconductors.

Wang et al. in [9] studied an important characteristic of GaN devices known as dynamic on-resistance parameter. It is shown that the on-resistance parameter value of the tested e-mode GaN devices is related to the amplitude of the applied gate voltage. In addition, experimental results presented in [9] illustrated that hard-switching operation can shift the threshold voltage of the device leading to further reduction in its on-resistance value. This phenomena, as well as the impact of other parameters such as ambient temperature on the on-resistance veriation were reported in [9] and [10]. Jones et al. [11] investigated the impact

TABLE I. THE CHARACTERISTICS OF THE CURRENTLY AVAILABLE GAN DEVICES IN THE MARKET

Part Number	Manufacture	Type	$V_{ds,max}$ (V)	$I_{d,max}$ (A)	Typ. R_{ds} (mΩ)	$V_{Gate,th}$ (V)	Qgate (nC)	Kelvin Pin	Package
TP65H050WSQA	Transphorm + Fujitsu	d-mode	650	35	50	4	9.3	No	TO-247
TP90H050WS	Transphorm + Fujitsu	d-mode	900	34	50	3.9	15	No	TO-247
IGO60R070D1	Infineon	e-mode	600	31	55	1.2	5.8	Yes	DSO-20-85
V22TC65S1A	VisIC	d-mode	650	100	22	6.8	4.3	Yes	SMD (custom)
GS66508B	GaN Systems	e-mode	650	30	50	1.7	6.1	Yes	SMD (custom)
GAN063-650WSA	Nexperia	d-mode	650	35.4	50	3.9	15	No	TO-247

of ambient temperature on the turn-on losses of GaN HEMTs. It was shown that the values of the turn-on losses are increased as the junction temperature rises. While the impact of the temperature on turn-on losses is negligible at low operating power, a significant increase in turn-on losses has been reported in [11] at the high supplied power close to the rated power of the device. In [2] and [12], the loss distribution in GaN HEMT devices were studid under hard-switching mechanism. An experimentally verified loss model was also proposed using PLECS software taking the temperature veriations into account.

Understanding the characteristics of GaN switches, such as switching loss and rise time is essential for high efficiency and power density system design and optimisation. Although the proposed models in the literature are accurate, they are highly dependent on other construction parameters such as the parasitic components, some of which are unknown. In addition, these models require excessive computational effort. Another shortcoming with the proposed loss models is that, they mainly focus on analysing the turn-on characteristic of GaN switches, while other dynamic characteristics such as the devices' rise time were ignored. In this paper, the dynamic characteristics of a commercially available GaN device including switching losses, rise time, and fall time are studied. The device evaluation is performed based on a dual pulse test (DPT) experiment. the DPT procedure and the test setup are presented with sufficient details. The dynamic performance of the device is then analysed and finally, a switching loss model is developed.

II. DUAL PULSE TEST CIRCUIT

A. DPT Procedure for the GaN Device Characterisation

DPT is a well-known test procedure for analysing the dynamic response of a semiconductor device. During the test, a single switch called device under test (DUT) is turned on and off repeatedly while the DUT's drain to source voltage waveform and drain current are measured simultaneously. The dynamic performance of the DUT will then be analysed based on the measured voltage and current waveforms. It is important to note that the parasitic elements existed in the circuit lead the circuit loss to be larger than the actual switching losses. They also influence other characteristics of the device such as rise time, fall time and voltage transients. Therefore, for accurate measurement of the device parameters, the DPT circuit should be designed similar to the real layout of the power converter.

Fig. 1 shows a schematice of the test circuit. The DUT switches an inductive current. The required second path for conducting the current is provided through an anti-parallel freewheeling diode connected across the load. Since the dynamic response of the anti-parallel diode affects the measured drain current, a fast high-voltage Si/SiC Schottky diode is proposed in [5], [8], [9] as anti-parallel diode across the load.

In the majority of power converter structures, the semiconductors are connected in several legs with two or more identical switches in each leg. These switches can have influence on the switching losses of each other. Therefore, adopting a parallel Schottky diode in DPT setup results in an inaccurate loss measurement due to the mismatch between switching speeds of the Schottky diode and the DUT device. In order to resolve this issue, it is recommended to utilise an identical device to the DUT in parallel with the load with its gate and source terminals are shorted [2]. In this configuration, the effects of the second switch on the switching losses of the DUT is considered leading to an accurate loss measurement.

The applied gate signal to the DUT and the voltage and current waveforms are illustrated in Fig. 2. As shown, the first

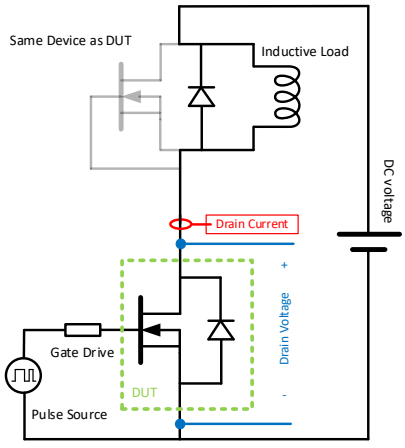

Fig. 1. Schematic of the DPT circuit used in this study

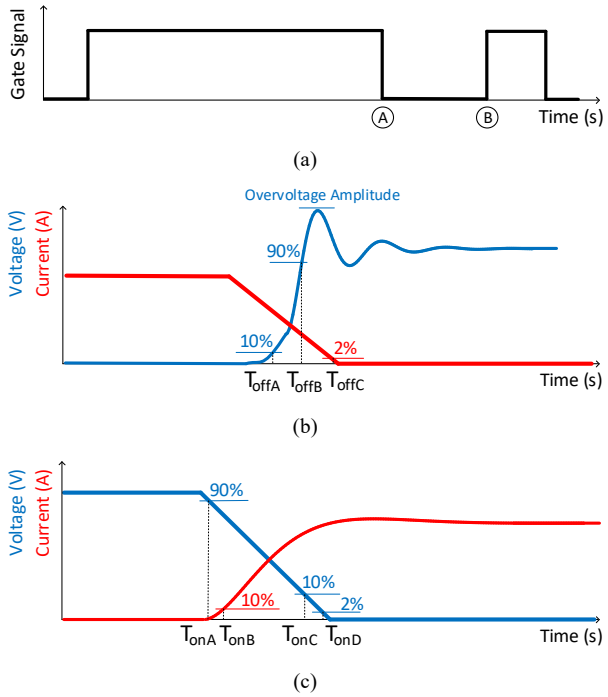

Fig. 2. A view of the DPT switching waveforms: (a) applied gate logic signal, voltage and current during (b) turn-off (c) turn-on periods

pulse allows the inductive current to rise to the required value and before the device is turned off. After a short time period (10 us), the DUT is turned on again for another short period i.e. 5 us. The device is then remained turned-off for a period of less than about 1 s to cool down and the temperature becomes stable at room temprature. The value of the turn-on and turn-off energy losses can then be calculated at points A and B, respectively.

B. Development of the Experimental Circuit Board

The selected GaN transistor is an IGO60R070D1 650V/31A e-mode GaN switch from Infineon Technologies. The switching device is chosen from Infineon CoolGaN™ e-mode series. It has a minimum breakdown voltage of 800 V and capable of conducting up to 20 A current at 100°C continuously. A Kelvin connection pin required for efficient gate driving at high frequencies is incorporated by manufacturer. The CoolGaN™ series has a unique gate structure that can be modeled by a parallel diode between the gate and source pins of the device [14]. Fig. 3 illustrates the gate drive configuration used in the GaN DPT circuit. The anode pin of this equivalent diode is connected to the gate pin of the device to limit the applied voltage across gate and source terminals to the diode forward voltage. Although this provides protection against overvoltage, it leads to continuous current-sinking while the device is turned on. As a result, a special gate drive mechanism is proposed by the manufacturer, as shown in Fig. 3, for efficient switching operation. The experimental DPT test setup is shown in Fig. 4. The tests were conducted with a 0.5 mH inductor as the load. The gate drive voltage was 8 V supplied from an isolated voltage source. The DC link voltage was connected to a set of parralled capacitors to generate a constant DC link voltage. The capacitor bank was constructed on a sepperate PCB and therefore not shown in the figure. However, a local 10 uF film capacitor with a low equivalnet series resistance was placed on the DPT board to ensure the stability of the DC link voltage. The DPT parameter values are shown in Table II.

TABLE II. MAIN DPT CIRCUIT DESIGN PARAMETERS

Parameter	Description	Value
R_{on}	Limits gate charching current peak	10 Ω
R_{off}	Turn-off resistor	1 Ω
C_{on}	Gate charging capacitor	3.3 nF
R_{ss}	Turn-on current steady-state resistor	470 Ω
V_{GS}	Gate drive voltage	8 V
$C_{DC\text{-}Link}$	DC link voltage	900 uF

III. EXPERIMENTAL CHARACTERISATION OF THE GAN DEVICE

The chosen GaN device was tested in a wide range of voltages and currents and the waveforms were obtained for each test case. Fig. 5 shows an example of the measured waveforms by DPT at 300 V and 10 A. The waveforms were then used to calculate the switching losses in the device. In addition, the device dynamic performance including rise time, fall time, and

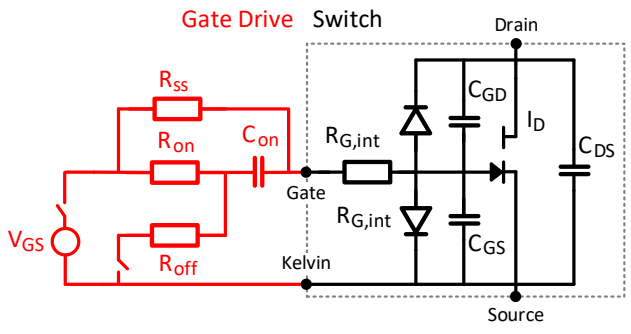

Fig. 3. The gate drive structure for the chosen CoolGaN™ device recommended by Infineon [14].

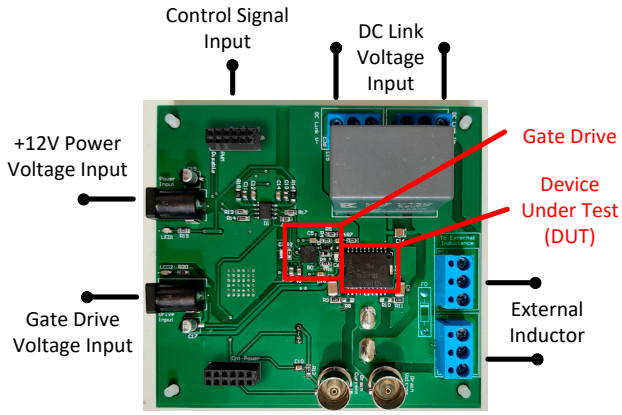

Fig. 4. Experimental DPT test setup used for GaN device characterisation

(a) (b)

Fig. 5. The DPT waveforms of voltage (yellow) and current (blue) at 300 V and 10 A at (a) Turn-off (b) Turn-on periods

peak voltage amplitude during turn-off period, were determined using the DPT results.

A. *Turn-off Loss Computation*

The value of the turn-off loss can be obtained as the integral of the product of the current and voltage waveforms during turn-off period. The integration starts from the point that the rising voltage reaches 10% of its final value i.e. T_{offA} in Fig. 2(b) and ends when the current falls to 2% of its starting value i.g. T_{offC} in Fig. 2(b):

$$E_{loss,off} = \int_{T_{offA}}^{T_{offC}} I_{Drain}(t)V_{DS}(t)dt \qquad (1)$$

The turn-off losses have been computed at various DPT voltages and currents and the results are shown in Fig. 6. As expected, the value of the turn-on loss rises when the applied current and voltage are increased.

B. *Turn-on Loss Computation*

Similar to the turn-off loss determination, the turn-on loss of a switch can be obtained by integrating the product of voltage and current waveforms during the turn-on period. The turn-on period starts from the point that the current reaches its 10% of the final value i.e. T_{onB} in Fig. 2(c) until the point that the voltage decreases below 2% of its starting value i.e. point T_{onD} in Fig. 2(c). Therefore, at a given applied voltage and current, the turn-on loss can be obtained from:

$$E_{loss,on} = \int_{T_{onB}}^{T_{onD}} I_{Drain}(t)V_{DS}(t)dt \qquad (2)$$

Fig. 7 illustrates the values of the turn-on losses obtained form the DPT experiments. Similar to the turn-off loss, the value of the turn-on loss is increased when the applied voltage and current are increased. Another important conclusion from the loss measurements is that the turn-on losses are substantially larger, by approximately 10 times, than the measured turn-off losses in the device. This may be due to the fact that the value of the voltage across the device is high and equal to the DC voltage at the beginning of the turn-on period leading the value of the product of the current and voltage to be higher than that of the turn-off period.

C. *Switching Rise Time and Fall Time*

Rise time is normally defined as the time taken for a signal to rise from 10% to 90% of its final value as illustrated in Fig. 2(b). Same definition is also adopted here in this study. It is important to note that the rise time of a device is referred to the voltage signal only, since the value of the current is dependent on the nature of the load. The same concept is defined for fall time as the time required for the voltage across the DUT to fall from 90% to 10% of its starting value.

Figs. 8 and 9 show the measured values of the rise time and fall time, respectively, for a range of applied voltage and current values. As can be seen, fall time is mostly constant and independent of the operating voltage and current apart from the

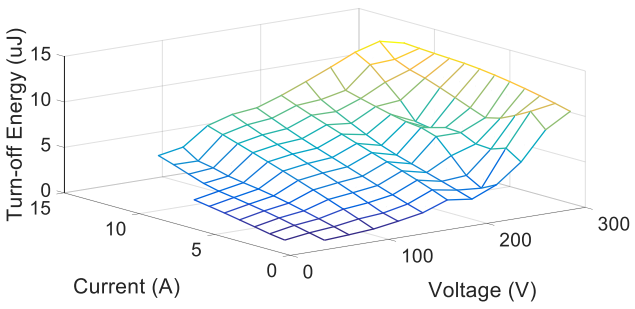

Fig. 6. Turn-off losses in the device obtained from experimental results

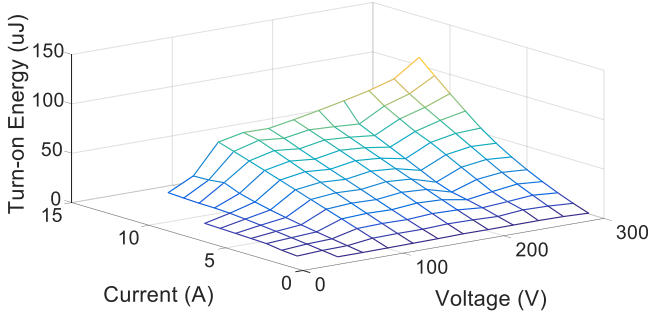

Fig. 7. Turn-on losses in the device obtained from experimental results.

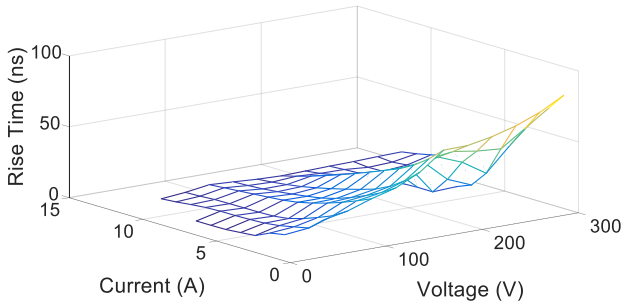

Fig. 8. The measured values of the rise time for the GaN device at various voltage and current levels.

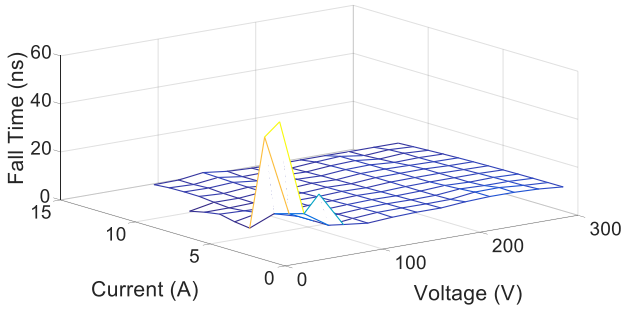

Fig. 9. The measured values of the fall time for the GaN device at variou voltage and current levels.

cases when the current and voltage values are lower than 4 A and 75 V, respectively. Nevertheless, the rise time increases gradualy by increasing the applied voltage and reducing the current in the circuit as can be seen in Fig. 8.

Since the value of the switching dead time is determined based on the switching dynamic characteristics of a device, the slow rise time can result in undesirable operation of the overall power converter at low-current operating regions. Therefore, special consideration is required for the low current operation to avoid undesirable performance such as distortion in the load voltage waveform and shoot-through occurence. The approximate values of the measured rise time and fall time for the currents higher than 7 A as the main operating region of the device are approximately 15 ns and 9 ns, respectively.

D. Peak Overvoltage During Turn-off Period

Unlike the MOSFET switches that benefit from an inherent resilient against transient overvoltage due to the avalanche characteristic of the body diode existed in its sturcture, GaN devices are sensitive to transient overvoltage since their drain to source breakdown voltage is close to their rated voltage. Therefore, applying a voltage to the device larger than the maximum allowable voltage can lead to a permanent failure of the device. The peak overvoltage incidents are frequent during turn-off periods and can be exacerbated in the presence of paracetic components and purly resistive loads. Fig. 10 shows the amplitude of the measured peak voltage seen across the DUT at turn-off interval. The overvoltage amplitude is dependent on the switching speed of the device as well as the load impedance value. As clear, by increasing the applied current, the peak amplitude of the voltage increases to the point at which increasing the currents higher than 13 A may cause a serious damage to the device. It is important to note that in the DPT setup used in this study, a snubber circuit is not utilised in order to examine the actual switching characteristics of the device, and to assess the overvoltage effects on the switching performance. This also leads to the conclusion that in an actual power converter system the failure of the snubber system can lead to distructive damage to the devices even at low operating currents.

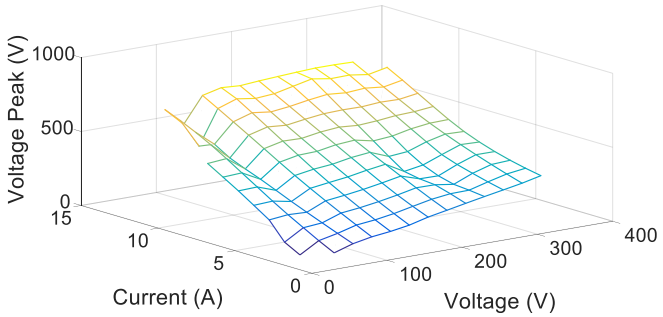

Fig. 10. The amplitude of the measured voltage peak across the DUT.

E. Turn-on and Turn-off Loss Models

It is a normal practice to adopt a curve fitting method to extend the DPT results to larger current and voltage ranges than the test schedule. Therefore, the device turn-off and turn-on values can be estimated for any given voltage and current values within the operating range. Fig. 11 shows the polynomial curve fitted to the measured turn-off results by using MATLAB curve fitting toolbox that can be expressed as:

$$E_{loff,fit}(v_{ds}(t), i_d(t)) = P_{00} + P_{10}\, v_{ds}(t) + P_{01}\, i_d(t) + P_{11}\, v_{ds}(t) i_d(t) + P_{02}\, i_d(t)^2 \quad (3)$$

The coefficients of the fitted curve provided by the MATLAB toolbox need to be tuned manually to enable curve fitting with acceptable accuracy. The coefficient values are determined and shown in Table III. The same procedure can be performed to obtain the turn-on loss parameters. Fig. 12 illustrates the fitted polynomial curve on the measured turn-on losses obtained using DPT experiments. The mathematical equation that represents the turn-on loss fitted curve is:

TABLE III. COEFFICIENT VALUES OF THE CURVE FITTING EQUATIONS FOR TURN-OFF (3) AND TURN-ON (4) LOSSES

Coefficient	Turn-off loss	Turn-on loss
P_{00}	1.84×10^{-1}	2.3×10^{-1}
P_{10}	1.25×10^{-2}	3.181×10^{-4}
P_{01}	8.37×10^{-2}	9.305×10^{-2}
P_{11}	6.724×10^{-4}	1.06×10^{-2}
P_{02}	4.64×10^{-2}	1.048×10^{-1}
P_{21}	-	3.626×10^{-5}
P_{12}	-	9.062×10^{-4}

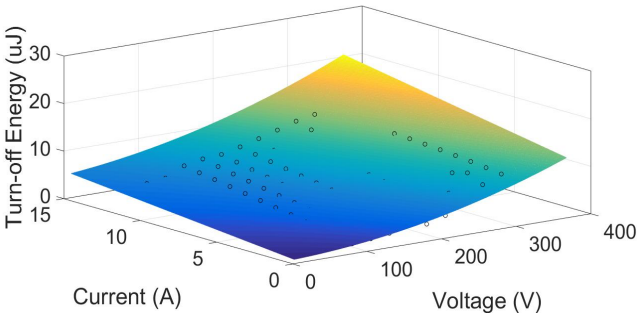

Fig. 11. The fitted curve of the turn-off loss results.

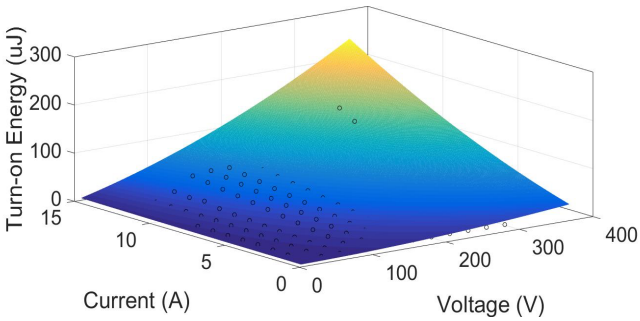

Fig. 12. The fitted curve of the turn-on loss results.

$$E_{lon,fit}(v_{ds}(t), i_d(t)) = P_{00} + P_{10}\, v_{ds}(t) + P_{01}\, i_d(t) + P_{11}\, v_{ds}(t) i_d(t) + P_{02}\, i_d(t)^2 + P_{21}\, v_{ds}(t)^2 i_d(t) + P_{12}\, v_{ds}(t) i_d(t)^2 \quad (4)$$

The coefficients are calculated and shown in Table III.

Equations (3) and (4) can then be used for estimating the switching losses of the system. The switching loss determination is essential for design optimisation of the power converter and its cooling system. Based on the estimated switching losses, the size and volume of the cooling system can be optimised to maximise the power density of the system.

IV. Conclusions

In this paper, the dynamic response of an e-mode power GaN switch was extensively analysed. In order to evaluate the performance of the device, an experimental dual pulse test (DUT) circuit was developed. The test results obtained from the DPT demonstrated that the fall time of the device is independent of the operating current and voltage values. However, the value of the device rise time is varied with the applied current and voltage. This can lead to a complexity in designing appropriate deadtime parameter for the GaN devices in a power converter operation. In addition, the experimental test showed that the value of the transient overvoltage can exceed the destructive breakdown voltage threshold of the GaN device even at a current level as low as the half of the rated current.

Based on the extrapolation of the DPT results, a switching loss model was developed to estimate the switching losses of the GaN device at various operating conditions with different supplied currents and voltages. The switching loss characterisation is a key requirement at the design stage for assessing the efficiency and reliability of the power converter as well as realising its cooling requirements for various applications such as automotive and photovoltaic systems.

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