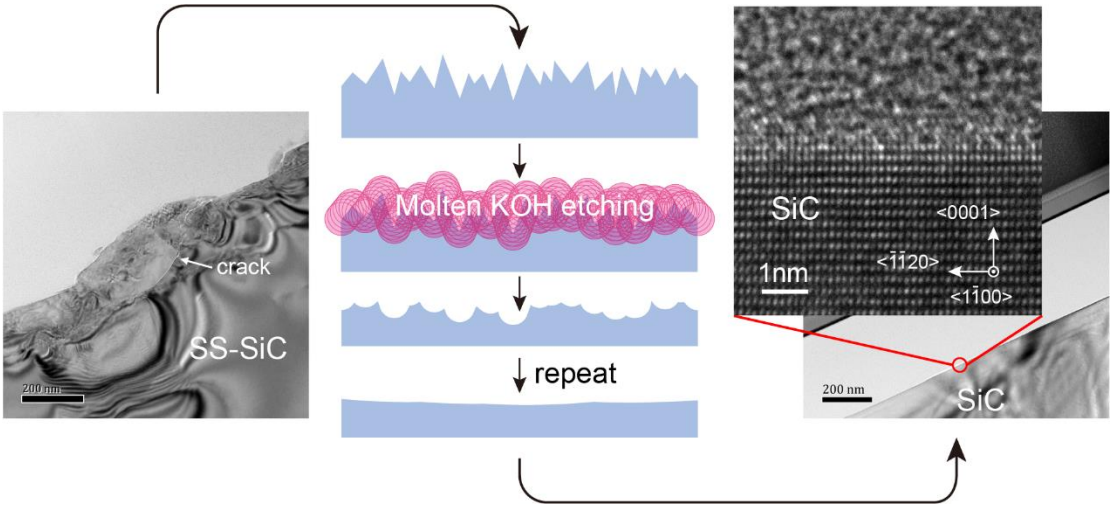
Highlights

- Molten KOH etching have been first applied to polishing sliced SiC.
- Sa roughness is reduced from 246.5 nm to 16.06 nm within 2 min of molten KOH etching.
- A damage-free surface can be obtained.
- Etching behaviors and mechanisms for dislocation spot is particularly studied.

Graphical Abstract



High efficient polishing of sliced 4H-SiC (0001) by molten KOH etching

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Abstract

Single-crystal silicon carbide (4H-SiC) is a promising third-generation semiconductor material because of its excellent electrical, mechanical and chemical properties. However, the high hardness of 4H-SiC makes it a typical difficult-to-machine material, which greatly restricts the development of SiC devices. In this work, molten KOH etching was first used to polish SiC. The perfect crystal surface and dislocation spots were studied separately. For the perfect crystal surface, a typical isotropic etching polishing behavior was observed. The speed of the polishing process was closely correlated with the temperature. An ultrafast polishing of sliced SiC was achieved, reducing the roughness from 246.5 nm to 16.06 nm within 2 min at 800 ℃, and all subsurface damage was removed, as demonstrated by TEM. For the dislocation spot, a relationship between the etch pits angle and temperature was found, making it possible to remove the influence of the dislocation spot by increasing the etch pits angle to approach 180°. This study shows that molten KOH etching could be a very promising SiC polishing method and deserves further research. We anticipate that this approach will be applicable to ultrafast polishing of SiC at the industrial scale.

Keywords

Single crystal SiC; Molten KOH etching; Polishing; Dislocation; Etch pits.

1. Introduction

As one of the most promising third-generation semiconductor materials, single crystal silicon carbide (4H-SiC) has attracted significant attention due to its excellent electrical, mechanical and chemical properties, and this material has been found to be especially suitable for producing devices that operate under high voltage, high frequency and high temperature conditions [1-3]. To fabricate electronic devices based on 4H-SiC, an atomic flatness and damage-free surface is essential. However, owing to its high hardness (Mohs hardness: 9.0-9.5) and high chemical inertness, SiC is one of the most difficult-to-machine materials in the world [4, 5]. How to obtain a smooth SiC surface efficiently without any damage remains a challenge.

To smooth SiC, a mechanical method will inevitably introduce new damage, such as scratches, subsurface-surface damage (SSD) and residual stress, to the sample [6, 7]. Meanwhile, chemical mechanical polishing (CMP) method generally have a low etching rate due to the excellent chemical inertness of SiC [8]. For highly efficient smoothing of sliced SiC wafers, electrochemical mechanical polishing (ECMP) method has been reported [9]. However, the efficiency of this process is greatly dependent on the doping concentration, which is not applicable for semi-insulating wafers. A pure chemical method could solve the problems that come with mechanical or electrical related polishing method. Among the various etchants employed for etching SiC, molten KOH etching is preferable due to its high selectivity and moderate operating conditions [10]. Compared with etchants based other alkali metals, potassium have relatively larger radius, therefore less likely to diffuse into the bulk SiC and cause contamination [11]. The applications of molten KOH etching to reveal dislocations in SiC have been extensively studied [8, 12]. As a form of pure chemical etching, no SSD is introduced during the etching process due to the zero normal stress applied to the surface [13]. Meanwhile, the etching speed can reach > 3 um/min, which is 1800 times higher than that of the conventional CMP method [14]. However, KOH has not been used to polish SiC due to the dislocation revelation effect. As molten KOH etching is considered the most convenient method to reveal dislocations in SiC, dislocation spots

on SiC will be preferentially etched and form a large etch pit and seriously increase the surface roughness, which are the main difficulties that hinder the polishing applications of molten KOH etching [15].

To address this challenge, we studied the etching behavior of dislocation in SiC. The development of etch pits requires that etching proceed faster in the direction of the dislocation than on the surrounding surface [16]. The higher etching rate along the dislocation could be attributed to the localized strain field, which implies excessive elastic energy that reduces the energy barrier of etching [17]. However, the strain energy of the dislocation will decrease with the increase of the temperature due to the reduction of the shear modulus [18]. Thus, the enhancement of the etching rate from the dislocation could decrease when the temperature increases and could result in a wider etch pit angle. We find that the angle of the etch pit has a positive correlation with temperature in the experiment. When the angle is close to 180°, the roughness damage from the etch pit can be neglected. Molten KOH etching of SiC at a very high temperature could solve the dislocation pit problem. Thus, we believe that KOH could be a very promising approach for fast polishing of SiC.

In this paper, we propose a novel polishing method for molten KOH etching of SiC. Sliced surface SiC (SS-SiC) with surface roughness (Sa) of 246.5 nm could be reduced to 16.06 nm within 2 min. As demonstrated by TEM, the SSD is completely removed, and only the lattice arrangement of SiC remains on the surface. The etching properties of a perfect crystal surface and dislocation spot are studied separately. For the perfectly crystal surface, the etching process contains three stages: roughing, polishing, and bossing. Typical etching holes with a spherical geometry cover the surface, implying that this is an isotropic etching process [19]. The trend of the first two stages follows the isotropic etching polishing (IEP) model Yi et al. presented, where the roughness first increases and then decreases with the increase in the radii of the isotropic etching holes [20]. The bossing stage emerges only at high temperatures (> 800 ℃) due to the small KOH vapor bubbles generated by the increased saturated vapor pressure. The speed of each stage is closely associated with the temperature. At higher temperatures, each stage runs faster and thus reaches the turning point earlier, which is

crucial for fast polishing. For the dislocation site, the etch pit angle increases with temperature, and at ~1200 ℃, the dislocation effect is minimized. The use of a high temperature allows the threshold of the shear modulus to be reached, which completely releases the strain energy in dislocation spots, thus eliminating the enhancement of the etching rate from dislocations [21]. However, under high temperature conditions, the bossing effect greatly increases the surface roughness. This method cannot directly replace CMP method at current stage, but it can serve as a highly efficient method to remove the SSD layer for SS-SiC and obtain a relatively smooth surface. Further study is needed to either eliminate the bossing effect or reduce the etch pit vanishing temperature to get a better polishing result.

2. Method

Commercially available sliced surface on-axis 4H-SiC (SS-SiC) wafers were used in this study. All experiments were conducted on the Si (0001) face, which is also the most commonly used face for electronic device applications. The SS-SiC wafer was cut into 10 mm * 10 mm chips for the convenient of experiments.

The etching rate generally shows an Arrhenius-type temperature dependence, so precision control of the temperature is needed [10]. Generally, the molten KOH etching process is carried out in a nickel crucible filled with KOH (GR, 95%, Macklin) that has been preheated to the target temperature. However, we found that over a high temperature range (>900 ℃), reactions occurred between nickel and molten KOH and the SiC sample was highly polluted by their reaction product. To overcome this problem, a crucible-less molten KOH etching method was developed, as shown in Fig. 1. A small sheet of solid KOH (~0.05 g) was directly placed on the Si face of the SS-SiC sample, and then, this sample stack was placed on top of an adiabatic stage to make it easier to grip. Meanwhile, the muffle furnace was preheated to the target temperature. After achieving the target temperature, the sample stack with the adiabatic stage was sent into the furnace. Solid KOH was quickly heated to the target temperature due to the small mass, forming a molten KOH droplet that covered the whole Si face of the SS-SiC chip, and etching reactions took place. This method provides the fastest approach to heat KOH to the target temperature without pollution from the crucible. After the etching reached the target time, the sample stack was removed from the furnace and directly cooled in the atmosphere; then, it was washed with ultrasonic vibration in deionized water. The etching temperature was set to 500 - 1200 °C, and the washing time was 0 - 30 min. The as prepared sample was then further characterized.

CLSM (Confocal laser scanning microscopy KEYENCE VK-X1000) was employed to observe the morphology and measure the etch pit angle. A white-light interferometer microscope (Taylor Hobson M112-4449-02 CCI HD) was utilized to measure the surface roughness (Sa) of the sample. Each sample was measured 8 times in random locations, and the measurement area for each time was 50 μm × 50 μm. After

excluding the maximum and minimum, 6 of these areas were counted to represent the roughness of the sample. AFM (atomic force microscope, BRUKER Dimension edge) in the tapping mode was used to study the detailed morphology of the sample. To identify the SSD of the sample before and after molten KOH etching, TEM (transmission electron microscope, FEI Tecnai F30) was used to investigate the SSD, and FIB (Focused Ion beam, FEI Helios 600i) was utilized to prepare the sample. A carbon layer and 3 Pt layers were coated on the sample before FIB cutting to prevent scattering ion beam damaging the surface layer of the sample.

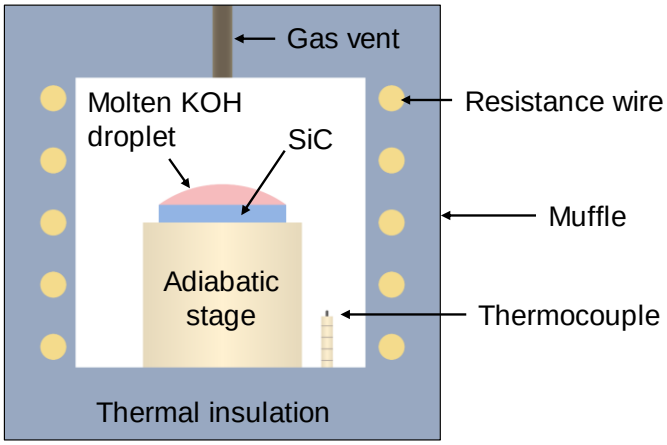

Fig. 1. Schematic diagram of the experimental setup for KOH etching.

3. Results and Discussion

3.1 Isotropic Molten KOH etching of SiC

Fig. 2a shows the typical morphology of the SiC surface after etching with KOH at 600 °C for 3 min. This AFM image shows a morphological intersection of the spherical surface, which implies that the etching process is isotropic. The cross-sectional profile of the red dashed line in Fig. 2a is shown in Fig. 2b. Compared with Fig. 2c, which is the profile of the original sliced SiC sample, the striking structures of the original sliced surface are removed, and the replacement is a link of arcs, suggesting that the original morphology can be fully removed by molten KOH etching and that an IEP-type surface remains. Fig. 2d shows the morphology change during isotropic etching, starting with a jagged structure on the SS-SiC surface, which implies that cracks and spikes were introduced during slicing of the SiC ingot. Isotropic etching occurs on every spot on the surface. As the etching process is isotropic, a red circle is used in Fig. 2d to imply that the etching range extends in every direction. The rest surface shows a line of intersecting arcs. The morphology change matches well with that shown in Fig. 2c and Fig. 2b. As we repeat the isotropic etching process several times, the surface becomes more and more flat. This matches with the typical morphology change of IEP provided by Yi et al. [20]. The predicted morphology change implies that KOH etching could be a promising approach for generating a smooth SiC surface.

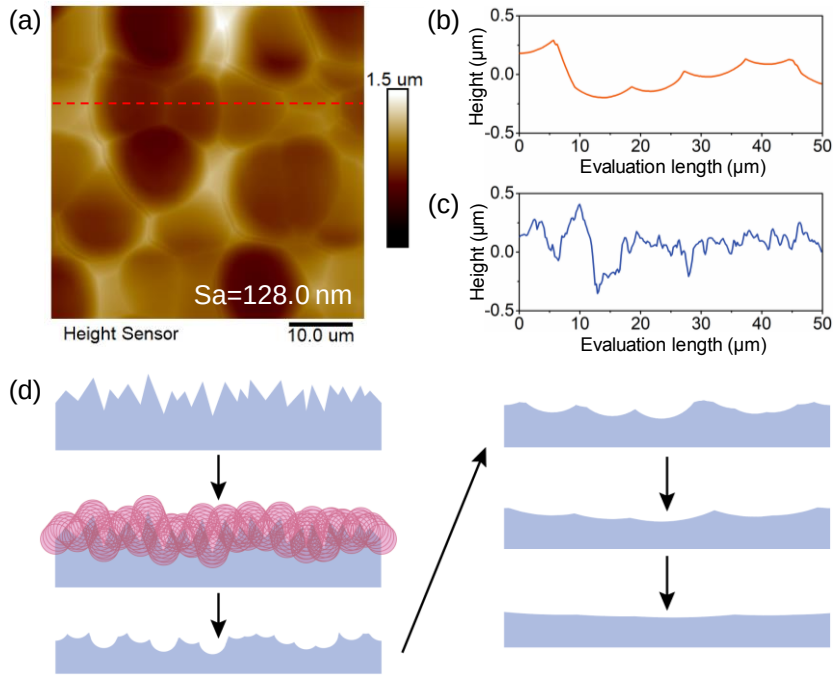

Fig. 2. (a) AFM image of the Si-face of the sliced 4H-SiC sample after 3 min of etching at 600 °C; cross sectional profile of: (b) the red dotted line in (a), (c) the Si face of SS-SiC and (d) the schematic of the isotropic etching polishing (IEP) process.

3.2 Etching characteristics under low temperature

Based on the mechanism of the morphology change in isotropic etching in 3.1, the resulting surface will be flatter when more materials are removed. According to the Arrhenius equation, the etching rate is exponentially related to temperature [22]. Thus, a higher temperature and longer time are expected to lead to a better smoothing result. The molten point of KOH under atmospheric pressure is 360 °C, while most studies of molten KOH etching of SiC are carried out in the range of 450 - 700 °C to prevent either underetching or overetching [15, 23, 24]. Considering the safety of the experiment and ensuring there is enough etching speed, we chose the most commonly used temperature range (500 - 700 °C) in the first stage of this study, and the duration times were from 0 - 30 min.

Fig. 3 shows the morphology change of SS-SiC etched at 500 °C for 0 - 30 min. The raw Si-face of the SS-SiC is shown in Fig. 3a. The cracks and spikes caused by the slicing process are shown, and the surface roughness (Sa) is 252.5 nm. After 3 min of

KOH etching, as shown in Fig. 3b, the Sa increased to 267.2 nm. This phenomenon is related to the opening of cracks in the SSD layers, which is also observed in the etching of fused silica using HF [25]. When the duration time exceeds this point, the roughness starts to gradually reduce, as observed in Fig. 3c-e. A surface filled with intersecting spherical surfaces with an expanding radius is observed, and the roughness drops to 58.1 nm for the 30 min sample, as shown in Fig. 3e. Fig. 3f shows the cross-sectional profile of Fig. 3a-e. The radius expansion of the etched spherical structure can be clearly observed, and the trend matches well the proposal presented in Fig. 2d. The isotropic smoothing mechanism using molten KOH etching is thus verified, and further studies were carried out.

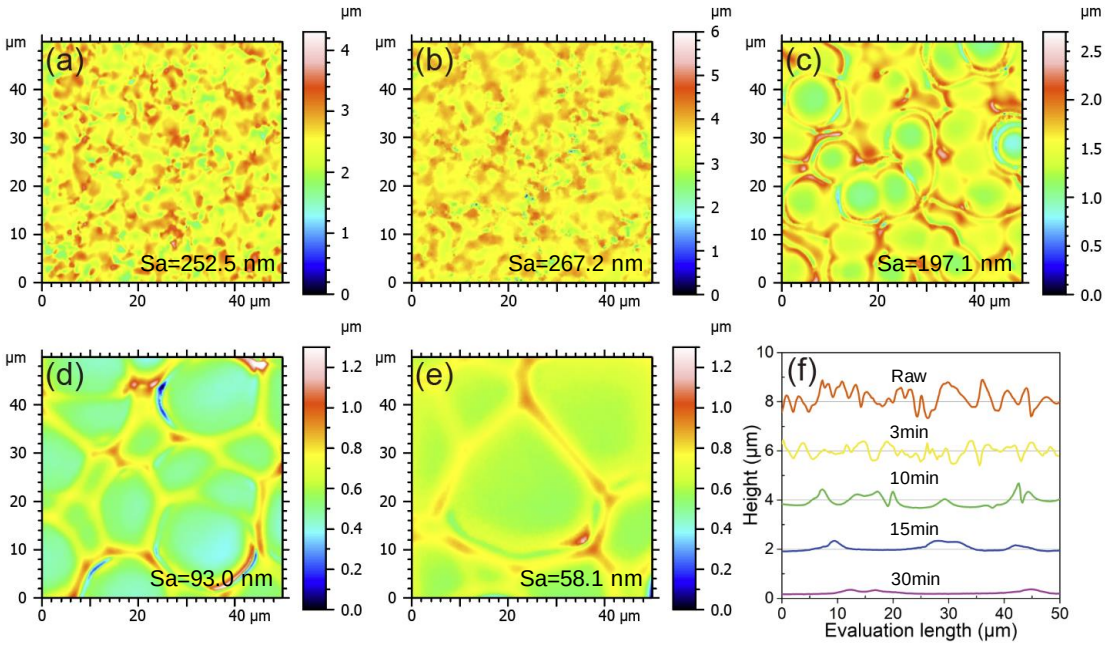

Fig. 3. White light interferometer image of the Si-face after etching at 500 °C for: (a) 0 min (the raw SS-SiC surface), (b) 3 min, (c) 10 min, (d) 15 min, (e) 30 min; (f) the cross-sectional profiles of the surface (a-e), respectively.

The roughness change of the etched surface at a temperature from 500 -700 °C and duration time from 0 - 30 min is shown in Fig. 4. For the 500 °C sample, which is also shown in Fig. 3, the roughness first increase as the crack opens and then reduces as the isotropic etching sphere increasers. The same trend was observed in the 550 °C sample. The roughness of the rising peak was achieved faster compared with that of the 500 °C

sample due to the increase in the etching rate. After reaching the peak point, the reduction was also faster with the increase of the temperature, and the effect of the etching rate increased, inducing an increase of the etching spherical expansion rate. For the sample at 600 °C and 700 °C, an increase in roughness in the early stage was not observed, possibly because the etching rate increased too fast that the peak achieved before our first picking point of 1 min. As the temperature further increased, the etching rate increased, leading to a more obvious increase of the smoothing process. For the 700 °C sample, the mean roughness was reduced from 246.5 nm to 48.7 nm within 1 min. With a further increase in duration time, the smoothing rate was reduced, which matches the IEP model presented by Yi et al. [20]. A minimum roughness of 19.2 nm was observed in the 700 °C 10 min sample.

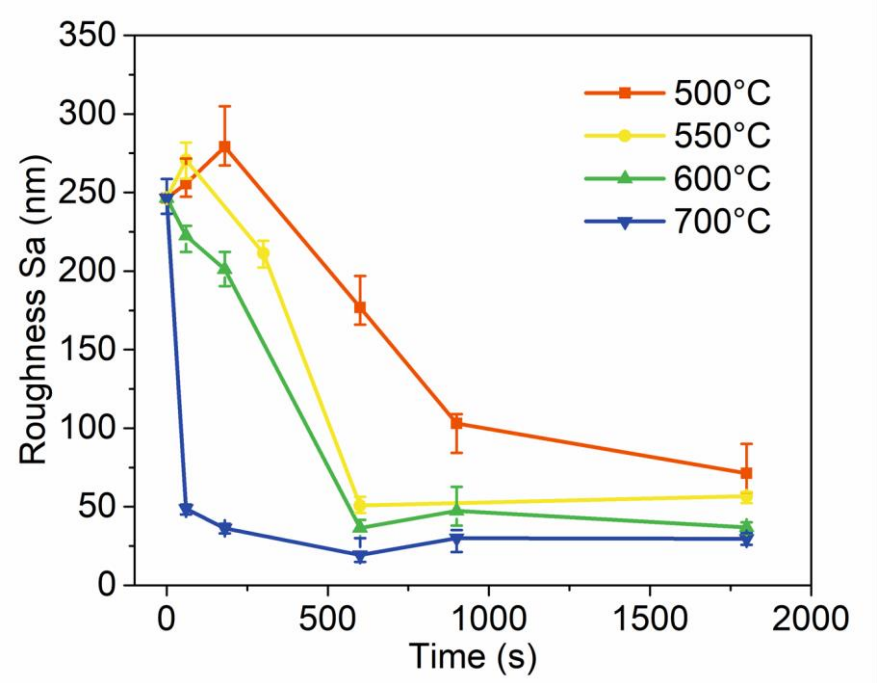

Fig. 4. Surface roughness of the Si-face of 4H-SiC after etching at 500 - 700 °C for 0 - 30 min.

In summary, two stage are revealed for molten KOH etching of SiC over a low temperature range (500 - 700 °C). The first stage is roughening, caused by the opening of cracks and SSD, which is common in the early stage of isotropic etching of materials with an SSD layer [26]. The second stage is polishing due to the expansion of the isotropic etching sphere. The speed of each stage depends on the temperature. To obtain

a faster polishing result, a higher temperature is needed. In addition, the etch pits of dislocations over the low temperature range heavily influence the overall roughness. Thus, the etching behavior of dislocation spots must be studied to obtain a better result.

3.3 Etching characteristics of dislocation

Molten KOH etching is regarded as the most common dislocation revelation method. Many etch pits of dislocations will form during the etching process, which strongly increases the overall roughness [27]. To obtain a better polishing result, the effect of the etch pits needs to be eliminated. Hartman et al. observed that when the temperature increased to > 1170 °C, a reduction (> 95%) of the dislocation density was observed in silicon because dislocation annihilation is unconstrained by crystallographic glide planes at high temperature [28]. Meanwhile, high temperature annealing is the most common approach for stress relaxation, which could reduce the level of dislocation [29, 30]. It is reasonable to presume that the revelation of dislocation etch pits is also highly related to temperature.

We first studied the relationship between the etch pit angle and the etching time. Fig. 6a-e shows an in-situ CLSM image of an edge dislocation found on the Si face of SiC, and Fig. 6f shows their cross-sectional profiles along each solid red line. As the duration time increases, the shape of the etch pits remains the same, but the pits increase in size. The etch pit angle remains the same. This result suggests that etch pits only get bigger and deeper as the duration time increases, while the angle remains unchanged. Thus, to minimize the effect of the etch pits, the etching time should be short.

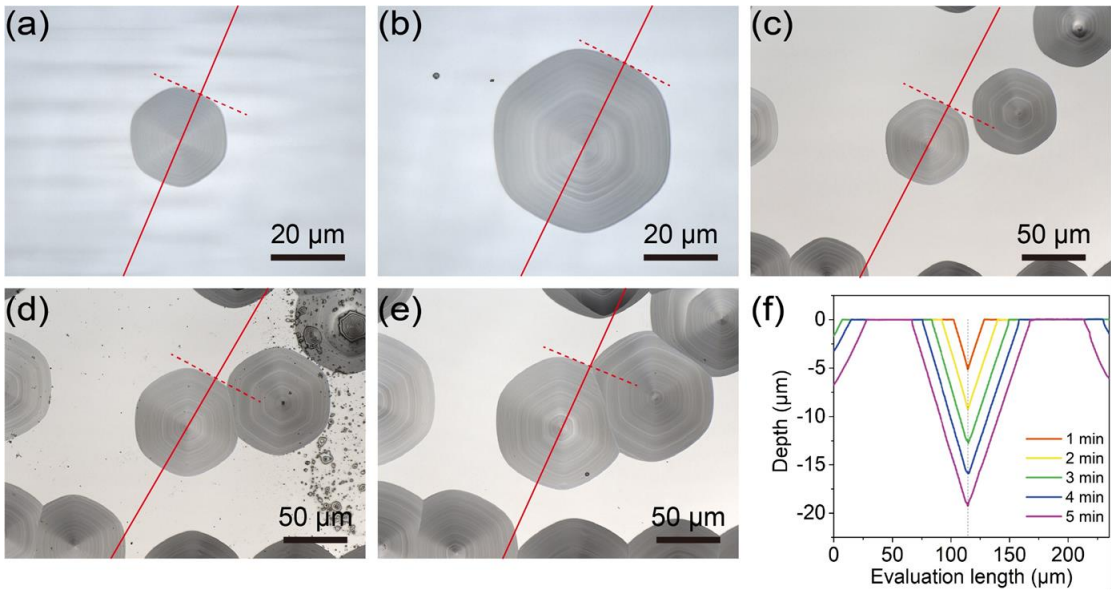

Fig. 5. In-situ CLSM image of an edge dislocation after etching at 550 °C for: (a) 1 min, (b) 2 min, (c) 3 min, (d) 4 min, (e) 5 min; (f) the cross-sectional profile of (a-e) along the solid red line. The angles are 138.5°, 137.8°, 137.0°, 137.4° and 138.1°, respectively.

To study the relationship between the etching temperature and the angle of dislocation of the pits, an in-situ study of edge dislocation etching at 500 ℃, 600 ℃ and 700 ℃ for 1 min is shown in Fig. 6. This study shows that with an increase in temperature, the etch pit angle increases. A more systematic diagram of the etching temperature and the etch pit angle is shown in Fig. 7. The etch pit angle of both edge dislocation and screw dislocation, which are the most influential types of dislocations that increase the surface roughness, was studied. Both types of etch pit angles increase with increasing temperature. The speculative mechanism for the increase of the etch pit angle with temperature is illustrated in Fig. 7b. We assume that the etching rate for the perfect crystal SiC surface is v_0, the etching rate along the horizontal direction is v_H, the dislocation effect-induced increase of the etching rate along the dislocation line is v_D and half of the etch pit angle is θ. tan(θ) can be expressed as Eq. 1:

$$\tan(\theta) = \frac{v_H t}{v_0 t + v_D t} = \frac{v_H}{v_0 + v_D} \qquad v_D > 0 \qquad (1)$$

As v_D is the increase of etching from dislocation, this parameter should be originated from the localized strain field, which contains elastic energy that reduces the etching energy barrier. v_D should be proportional to the energy associated with dislocation E_D, which is expressed in Eq. 2 and Eq. 3 [17]:

$$v_D\ (screw) \sim E_D(screw) = \frac{Gb^2}{4\pi} ln\left(\frac{r}{r_0}\right) \quad (2)$$

$$v_D\ (edge) \sim E_D(edge) = \frac{Gb^2}{4\pi(1-\nu)} ln\left(\frac{r}{r_0}\right) \quad (3)$$

where G is the shear modulus, b is the deformation distance of dislocation, r is the radius from the dislocation center, r_0 is the radius of the dislocation central core and ν is Poisson's ratio. From Eq. 2 and Eq. 3, we can find E_D is proportional to the shear modulus of SiC. According to the mechanical threshold stress (MTS) model, the shear modulus will decrease with the increase in temperature [21]. Thus, E_D and v_D will simultaneously decrease with temperature. From Eq. 1, we find that tan (θ) increases when v_D decreases. Meanwhile, when v_D becomes 0, the etching shape is represented by the red dotted triangle in Fig. 7b. No etch pits remain on the surface. The effect of dislocation is eliminated. It is reasonable to assume that the increase of the etching rate from dislocation will also disappear when the temperature is high enough. Thus, a high temperature is needed to eliminate the effect of etch pits.

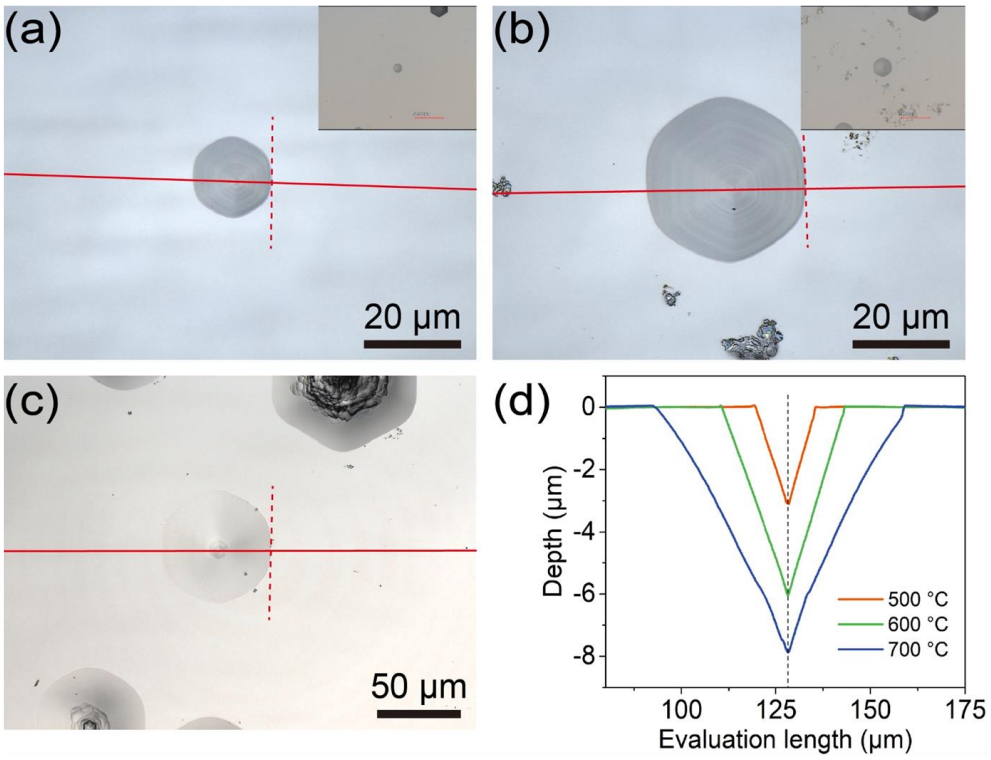

Fig. 6. In-situ CLSM image of an edge dislocation after etching for 1 min at: (a) 500°C, (b) 600 °C, (c) 700 °C; (d) the cross-sectional profile of (a-c) along the solid red line. The angles are 137.8°, 139.0° and 153.9°, respectively.

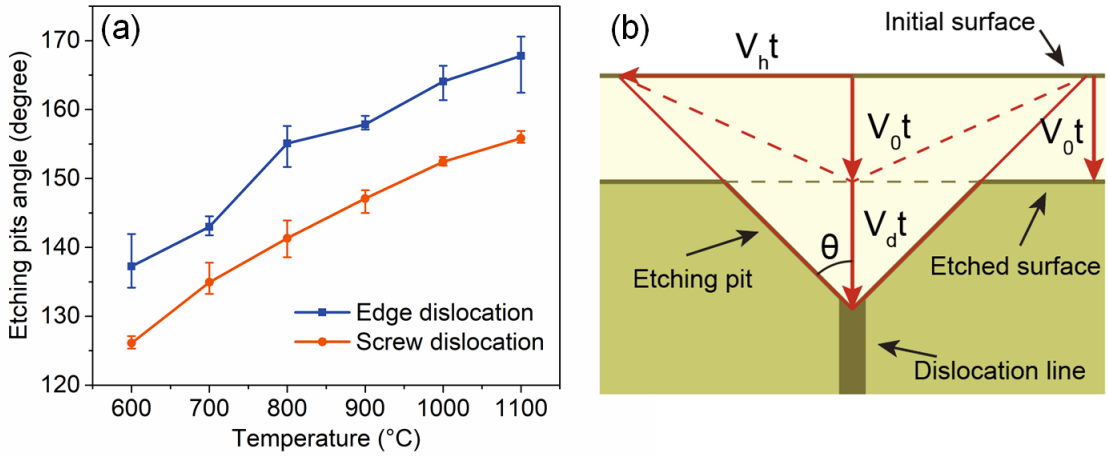

Fig. 7. (a) The relationship between the etch pit angle and the etching temperature for edge dislocation and screw dislocation after etching at 600 °C - 1100 °C for 2 min, and (b) the schematic of the etch pit formation.

3.4 Etching characteristics under high temperature

To prove our assumption regarding the temperature around the dislocation angles, we performed a set of experiments comparing the morphologies of SiC etched at high temperature (1200 °C) and low temperature (700 °C) for the same duration time (3 min), and the results are shown in Fig. 8. The 700 °C experiment is shown in Fig. 8a, where large etch pits of dislocations can be clearly identified. The dominant dislocation type is edge dislocation. The rest of the perfect crystal surface only shows the intersection of spherical surfaces. The 1200 °C sample is shown in Fig. 8b for the same magnification, and the results match our prediction. No large dislocation etch pits were observed, suggesting that the etching enhancement from the dislocation effect had disappeared. Only very small hexagonal etch pits were found, which might have been caused during the cooling process, when the temperature goes through a low temperature range for a short period of time, inducing low temperature etchings that could reveal dislocations. This shows high temperature can eliminate the effect of dislocations. However, many circular boss structures were also formed on the high temperature sample. One of the boss structures is shown in Fig. 8c, and the cross-sectional profile along the red dotted line and a 3D image are shown in Fig. 8d. This is a typical boss structure with a slash side wall. The height of this structure is ~1.64 μm, which strongly influences the surface roughness. The forming mechanism of the boss structure is illustrated in Fig. 8e. When the temperature is near the boiling temperature of molten KOH, many vaporized KOH bubbles are generated due to enhanced thermal fluctuation [31]. The bubbles that attach to the SiC surface prevent the spot inside the bubble from contacting in the presence of the surrounding molten KOH. Owing to the large difference in the reactant flux in the vapor and liquid states, the etching reaction in KOH vapor is much slower than that in molten KOH [32, 33]. The etching speed inside the bubble is slower than that in the surrounding SiC, which is in good contact with molten KOH. Thus, a boss structure is formed on the surface due to the bubble effect.

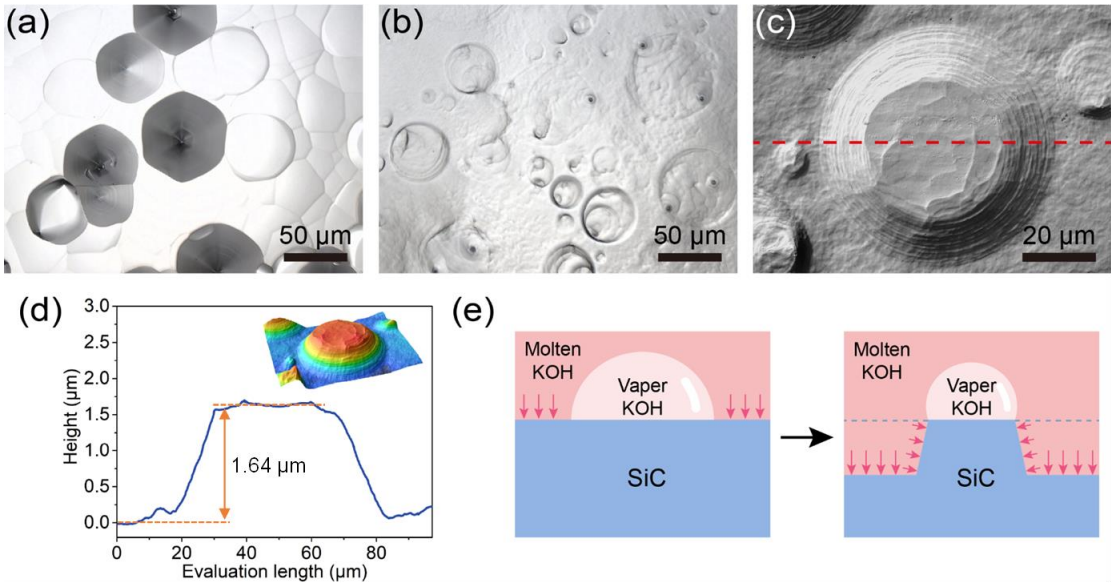

Fig. 8. CLSM image of the Si face of 4H-SiC after etching at (a) 700 °C for 3 min and (b) 1200 °C for 3 min. (c) A higher magnification of the sample in (b). (d) Cross sectional profile along the red dotted line in (c). The insert is the 3D image of (c) and (e) the schematic of the boss structure formation.

A set of experiments to determine the etching properties over a high temperature range (800 - 1000 °C) were carried out, and the results are shown in Fig. 9. The typical change shown in the morphology of the sample etched at 1000 °C for 15 s - 10 min is provided in Fig. 9a-e. From 15 s – 30 s, the morphology change looks like the change observed in Fig. 3c-e, possibly due to the temperature of KOH not having reached the target temperature. Thus, the change in morphology shows the characteristics of low temperature etching. After 1 min, the morphology becomes different. Although the surface roughness remains relatively low (~22 nm), many randomly distributed small protrusions are formed on the surface. When the duration time exceeds 10 min, the roughness dramatically increases. Many round boss structures form on the surface due to the bubble effect. The roughness change for temperatures from 800 - 1200 °C and duration times of 0 - 10 min is shown in Fig. 9f. The roughness changes generally occur in three stages: 1. When SS-SiC first contacts molten KOH, many subsurface cracks open, and the roughness increases. This phenomenon could be observed in the 800 and 900 °C sample. For a sample at a higher temperature, this process may occur too quickly

to be observed. It completed within 15 s, which is shorter than the shortest duration time in our experimental set. 2. When the roughness reaches the peak point, it quickly decreases due to the IEP effect. The polishing speed is closely related to the temperature, which determines the etching rate of the isotropic etching process and thus determines the expansion rate of the radius of the etched spherical surface. 3. When the roughness decreases to its lowest point, it will remain almost unchanged over the low temperature range. However, for a high temperature sample (≥ 800 °C), the bubble effect will gradually occur, causing the roughness to increase. The rate of increase is also determined by the temperature. The higher the temperature, the nearer the sample will be to boiling, and a strong bubble effect will cause the roughness to rapidly increase. The roughness of the final condition when the bubble effect is saturated is also determined by the temperature, which determines the frequency and size of KOH bubbles emerging on the surface. To avoid the dislocation effect, a high temperature is needed, while too high of a temperature will lead to the bubble effect. Thus, the optimized condition is in between. In this work, a Sa roughness of 16.06 nm is achieved for the sample etched at 800 °C for 2 min from SS-SiC with a Sa roughness of 246.5 nm. The material removal rate (MRR) is under this condition is estimated using the differential-weight method. Using the density of 3.21 g/cm^3, the MRR is approximated to be 5.87 μm/min, which is much higher than the K^+ ion diffusion rate [11]. This can dispel the concern of K^+ contaminate the bulk SiC.

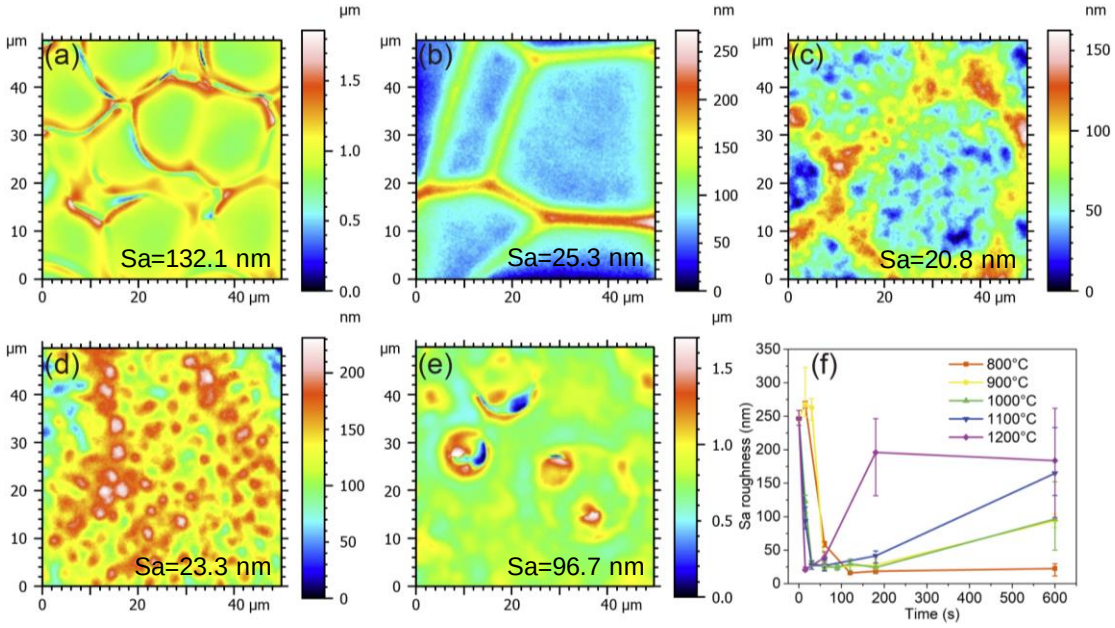

Fig. 9. White light interferometer image of the Si-face after etching at 1000 °C for (a) 15 s, (b) 30 s, (c) 1 min, (d) 3 min, (e) 10 min; (f) the surface roughness of the Si-face of 4H-SiC after etching at 900 - 1200 °C for 0 - 10 min.

To study the SSD and further evaluate the polishing effect of the etching process, TEM images of the cross sections of the SS-SiC and the sample with the best polished effect (800 ℃, 2 min, Sa = 16.06 nm) are provided in Fig. 10. To avoid the damage introduced by the FIB sample preparation process, 1 layer of carbon coated by a Marker pen and 3 layers of Pt (coated by magnetron sputtering, electron beam deposition and ion beam deposition, respectively) were deposited on the surface as a protection layer. Fig. 10a shows SS-SiC, and two defined regions can be observed. Immediately beneath the ground surface is the first highly deformed region, which has a depth of ~ 200 nm. This region contains a high density of dislocations. Many cracks introduced during the slicing process appear in this region [34]. The second region below is lightly deformed with lower density of cracks and dislocation. The SAED (selected area electron diffraction) pattern of spot 1 is shown in Fig. 10b. Although no full halo ring could be recognized, suggesting that SS-SiC did not have full amorphization, the strongly twisted pattern indicates that the crystal structure has undergone a serious deformation [35]. This kind of elongated spot is also observed in cold rolling metal, indicating great interior stress [36]. Fig. 10c shows the surface after polishing. The carbon and Pt

protection layer can be observed, ensuring no additional damage will be induced by FIB. The surface of SiC becomes very flat, and the two deformed layers are removed. The stripes observed in the SiC part are interference fringes caused by the bending of the TEM sample due to FIB processing [35]. The SAED pattern of spot 2 in the insert shows a typical diffraction pattern along the [0-110] zone axis of 4H-SiC, suggesting that all the damage and deformation are removed and that only single crystal 4H-SiC is left [37]. To further confirm the removal of SSD, a HRTEM image was taken of the SiC surface. The result in Fig. 10d coincides with the (1-100) face of 4H-SiC. A regular crystal structure is observed in the interface, suggesting the thorough removal of the SSD layer. The TEM results provide strong evidence that molten KOH etching can fully remove the SSD layer and obtain efficiently smooth SiC.

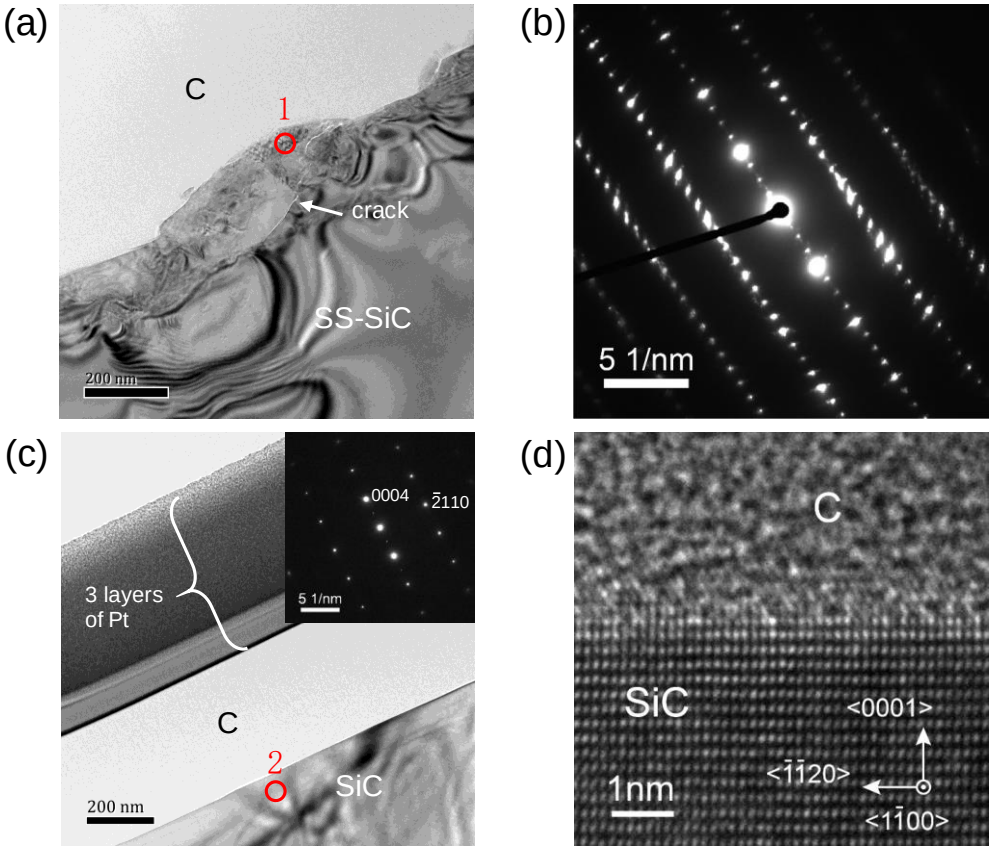

Fig. 10. (a) The TEM image of the SS-SiC sample, (b) the SAED pattern of spot 1 in (a), (c) TEM image of the sample after 2 min KOH etching under 800 ℃, the insert is the SAED of spot 2; (d) the HRTEM of (c).

4. Conclusions

A highly efficient flattening method for SS-SiC using molten KOH etching is proposed in this study. A roughness reduction from 246.5 nm of SS-SiC to 16.06 nm within 2 min is achieved using molten KOH etching at 800 °C and the MRR is estimated to be 5.87μm/min. As confirmed by TEM, all the SSD layers are removed, and only a perfect crystal structure remains after etching. The etching behaviors of SiC at low temperature and high temperature are studied in detail. When SS-SiC was etched at low temperature, it shows the typical characteristics of isotropic etching, which makes it possible to be a polishing method via the IEP mechanism. When etched at high temperature, the bubble effect due to the change in the saturated vapor pressure urgently demands the polishing effect. However, the disappearance of the dislocation effect requires a higher temperature and shorter etching time. At current stage, this method cannot directly replace the CMP method, but it can serve as a competitive alternative for grinding, lapping and mechanical polishing and is promising to be applicable to the industrial field. Meanwhile, it can remove the SSD layer for SS-SiC sample efficiently, and obtain a relatively smooth surface. We anticipate that better results can be achieved by inhibiting the bossing effect while increasing the temperature as much as possible.

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Declaration of interests

☒ The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

☐The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Credit Author Statement

Yi Zhang: Performing the experiments and data collection and analysis; Writing the manuscript.
Hongyingnan Chen: Performing the experiments and data collection; Writing the manuscript.
Dianzi Liu: Discussion about the results and revision of the manuscript.
Hui Deng: Supervision of the study and revision of the manuscript.